

COMPAL CONFIDENTIAL

COMPAL P/N :
PCB NO : LA-1761
Revision : 2.0
DATE :

LA-1761 Schematics Document
uFCBGA/uFCPGA Northwood

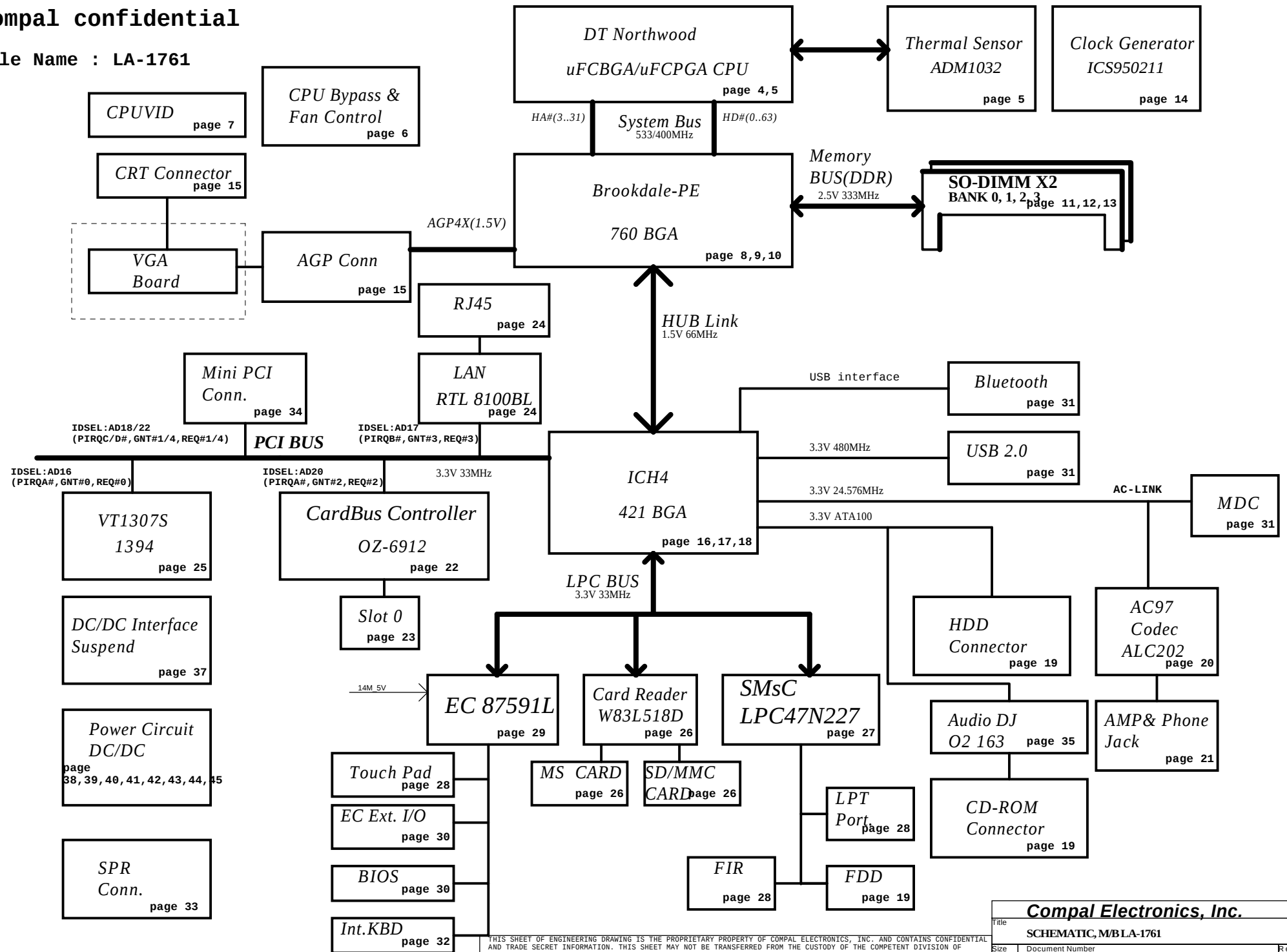
2003-03-12
REV: 2.0

Compal Electronics, Inc.		
Title		
SCHEMATIC, M/B LA-1761		
Size	Document Number	Rev
	401248	2A
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SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK

Power Managment table

Signal State	+3VALW +5VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	PCB Rev	CHIPS Rev
SST-Build	0.1	
PT-Build		
ST-Build		
QT-Build		

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+ -0.05PF	+ -0.1PF	+ -0.25PF	+ -0.5PF	+ -1PF	+ -2%	+ -3%	+ -5%

K	M	N	P	Q	V	X	Z	
+ -10%	+ -20%	+ -30%	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	

SMBUS Control Table

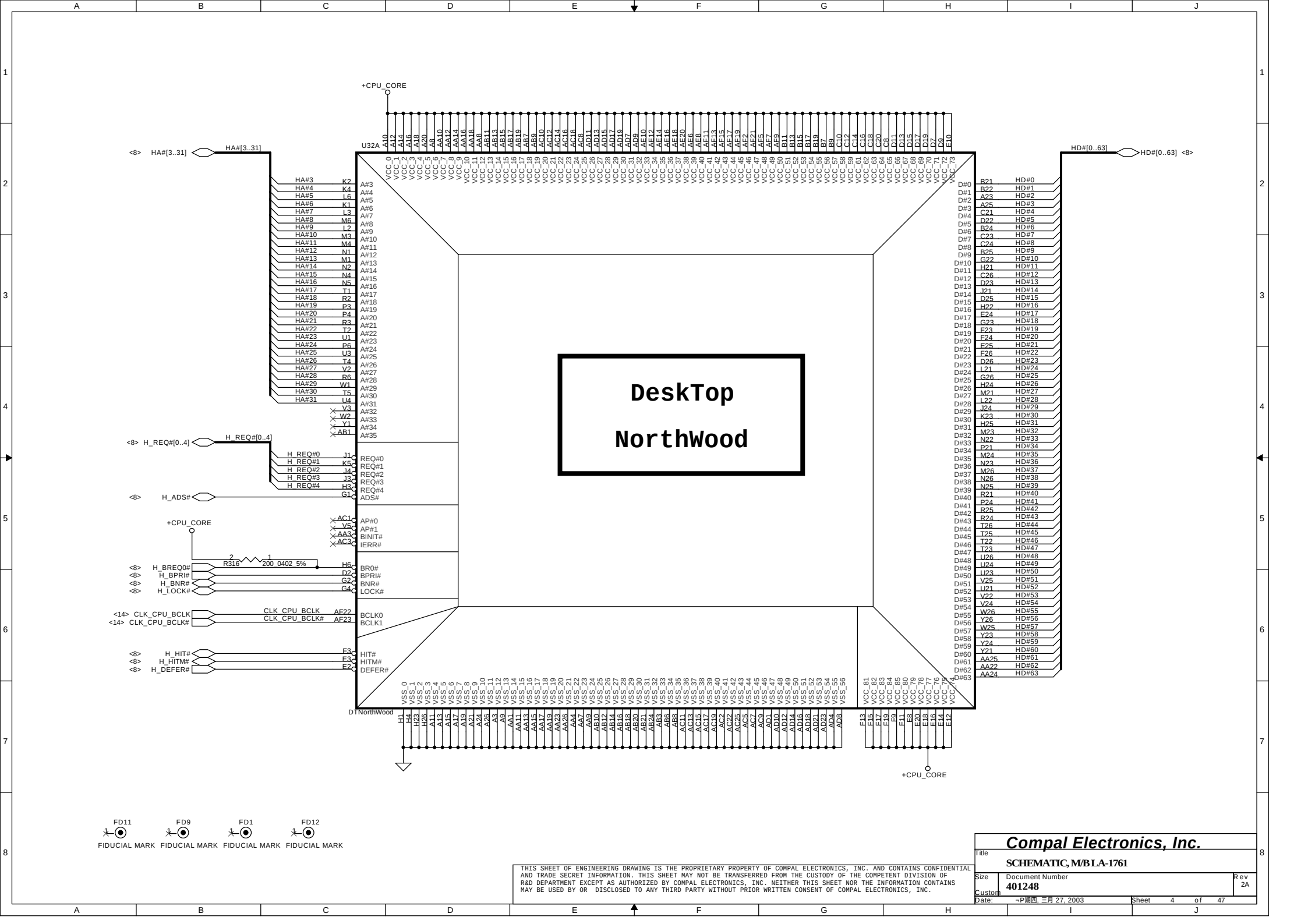
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (U43)	THERMAL SENSOR (U91)	SODIMM	CLK CHIP	MINI PCI
SMB_EC_CK1 SMB_EC_DA1	NS 87591	✓	✓	✓ (1010)	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	NS 87591	✗	✗	✗	✓	✓	✗	✗	✗
SMB_CLK SMB_DATA	ICH4	✗	✗	✗	✗	✗	✓	✓	✓

NOTE1:

@XX : Depop component

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DeskTop
NorthWood

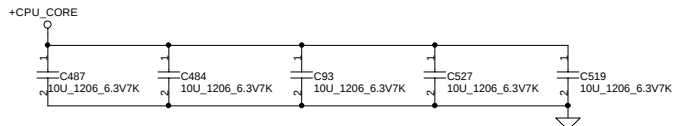
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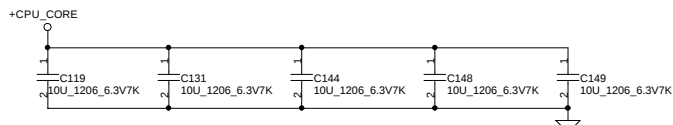
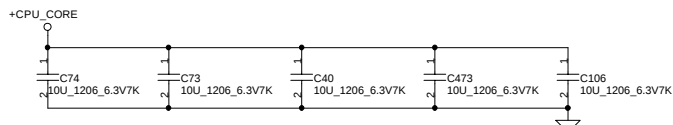
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

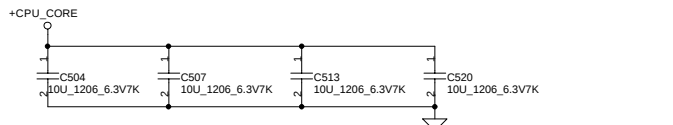
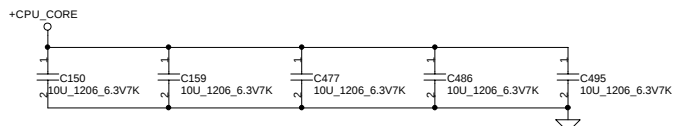
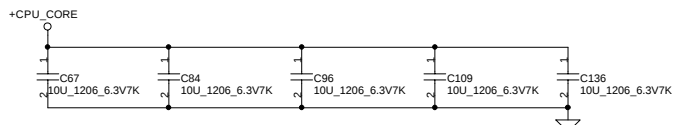
Please place these cap in the socket cavity area



Please place these cap on the socket north side



Please place these cap on the socket south side



Layout note :

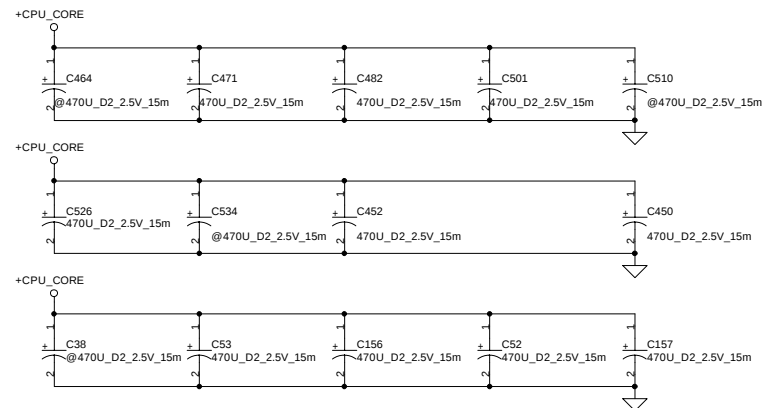
Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:

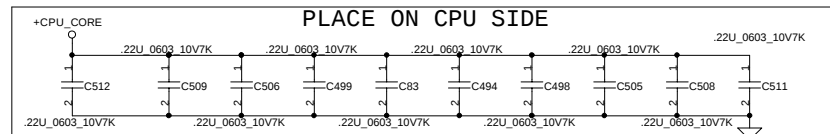
ESR total=0.75m ohm
C total=6350uF

For Mobile's CPU:

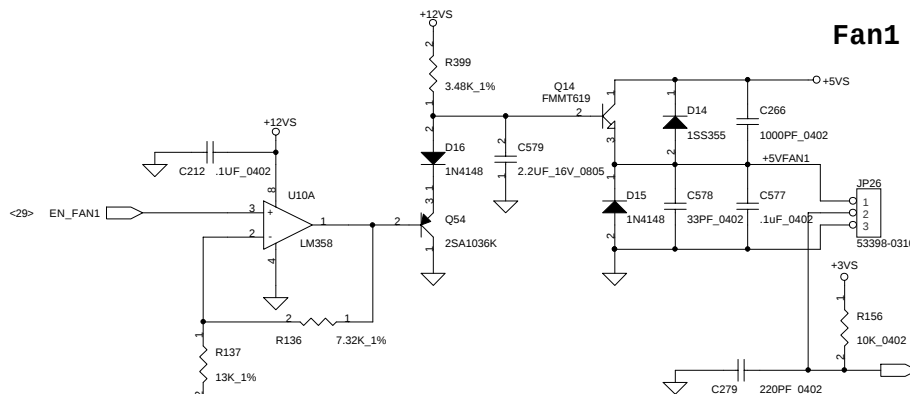
ESR total=1.875m ohm
C total=2590uF



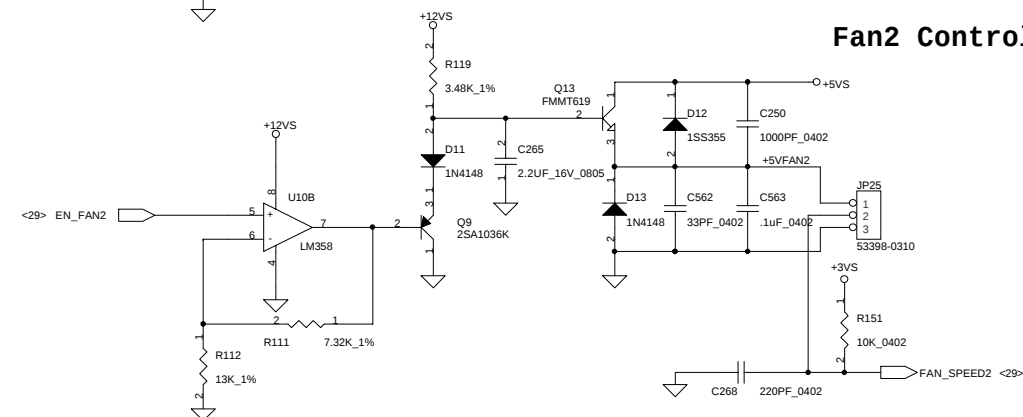
PLACE ON CPU SIDE



Fan1 Control circuit



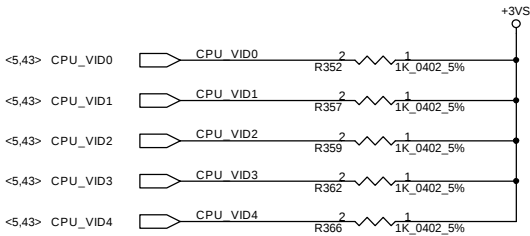
Fan2 Control circuit



Compal Electronics, Inc.

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	Desktop CPU				
VID	4	3	2	1	0
VCC					
1.750V	0	0	1	0	0
1.700V	0	0	1	1	0
1.650V	0	1	0	0	0
1.600V	0	1	0	1	0
1.550V	0	1	1	0	0
1.500V	0	1	1	1	0
1.450V	1	0	0	0	0
1.400V	1	0	0	1	0
1.350V	1	0	1	0	0
1.300V	1	0	1	1	0
1.250V	1	1	0	0	0
1.200V	1	1	0	1	0
1.150V	1	1	1	0	0
1.100V	1	1	1	1	0
1.050V	X	X	X	X	X
1.000V	X	X	X	X	X
0.975V	X	X	X	X	X
0.950V	X	X	X	X	X
0.925V	X	X	X	X	X
0.900V	X	X	X	X	X
0.875V	X	X	X	X	X
0.850V	X	X	X	X	X
0.825V	X	X	X	X	X
0.800V	X	X	X	X	X
0.775V	X	X	X	X	X
0.750V	X	X	X	X	X
0.725V	X	X	X	X	X
0.700V	X	X	X	X	X
0.675V	X	X	X	X	X
0.650V	X	X	X	X	X
0.625V	X	X	X	X	X
0.600V	X	X	X	X	X
VRM output off	1	1	1	1	1

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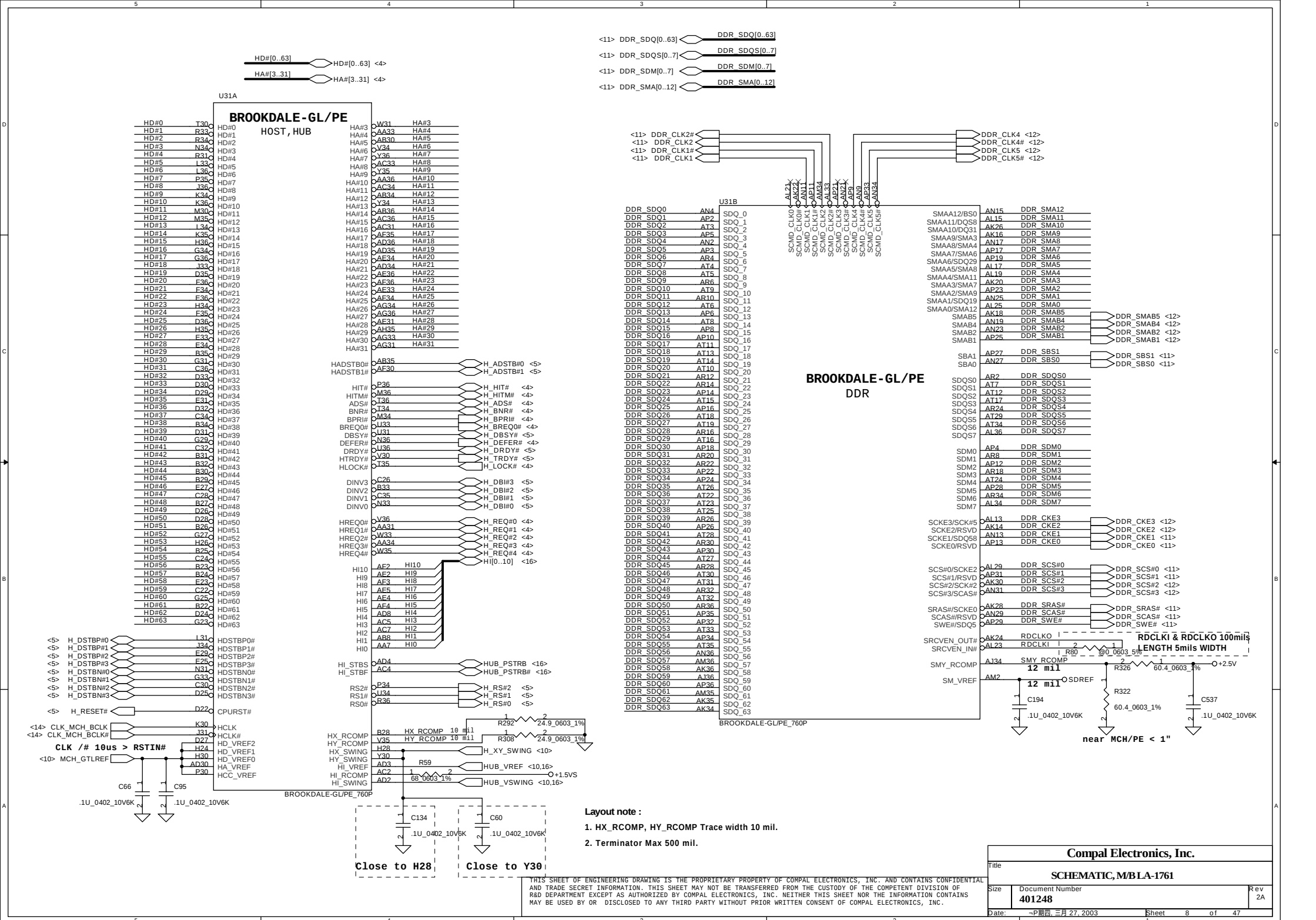
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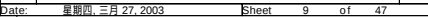
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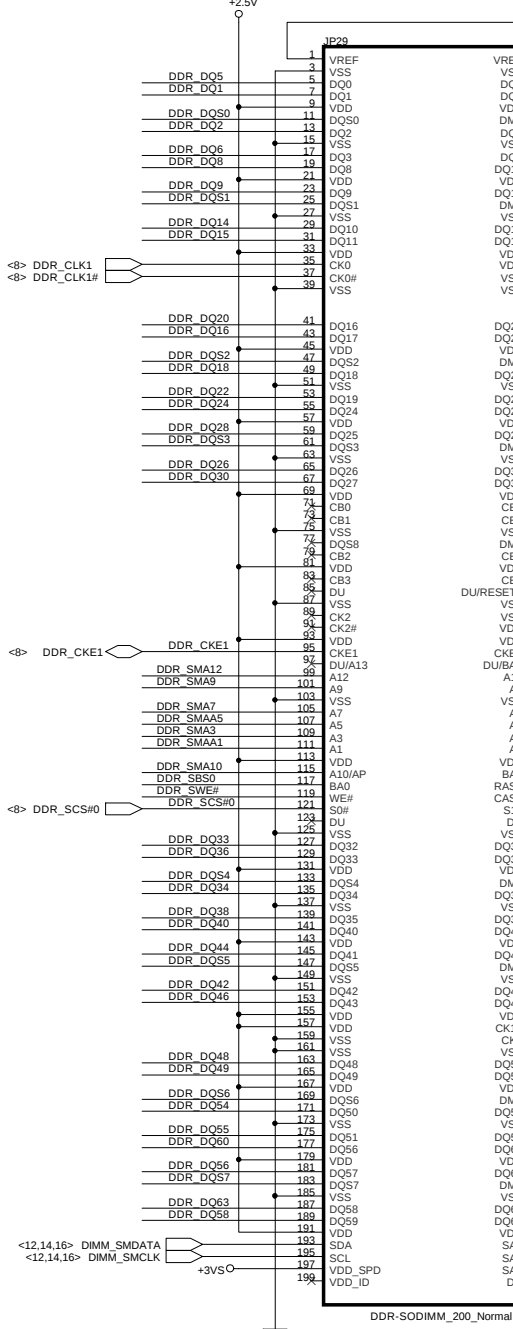
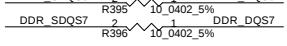
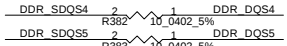
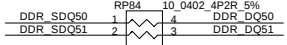
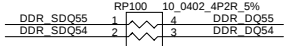
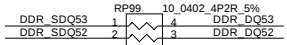
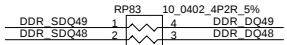
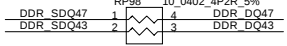
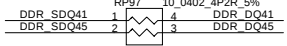
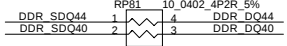
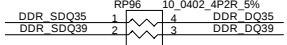
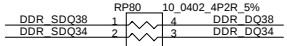
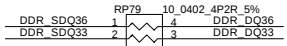
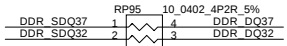
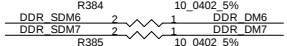
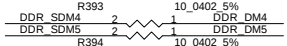
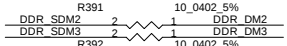
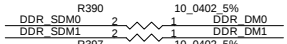
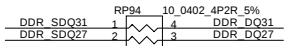
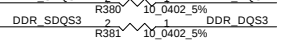
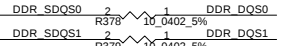
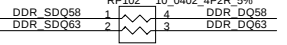
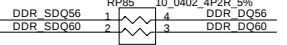
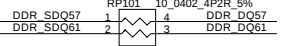
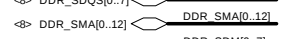
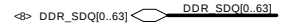
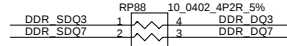
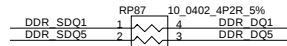
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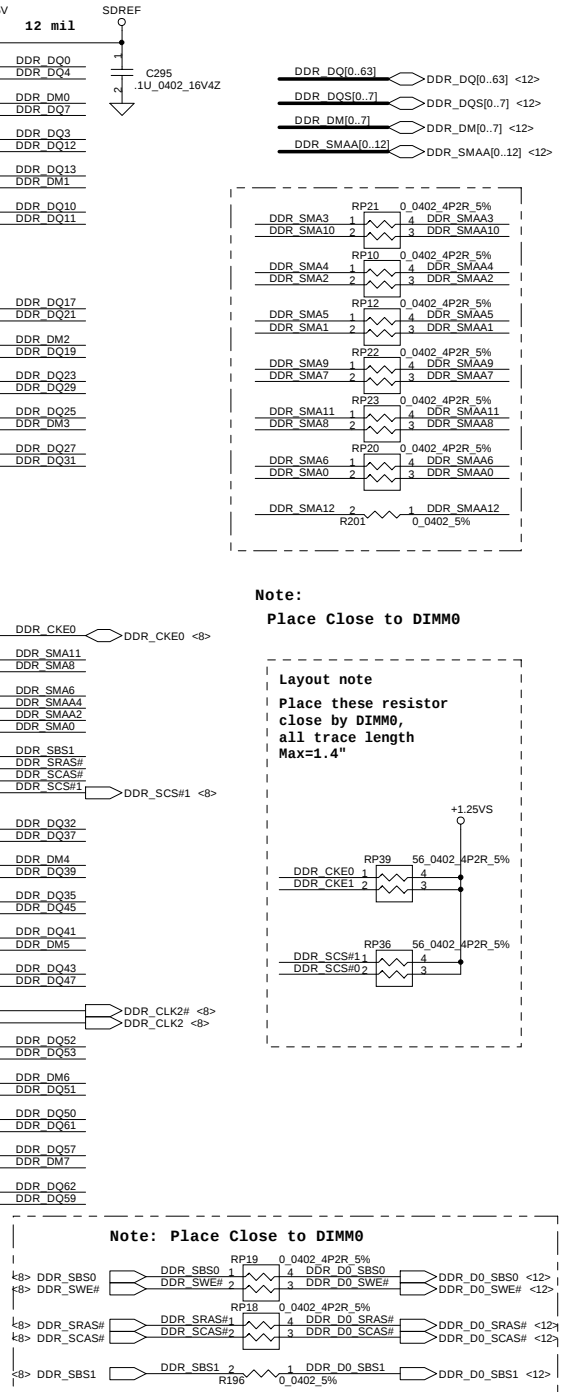
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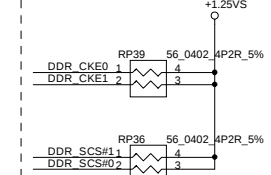


Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

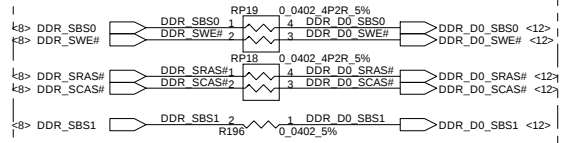


Note:
Place Close to DIMM0

Layout note
Place these resistor
close by DIMM0,
all trace length
Max=1.4"

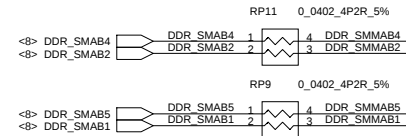
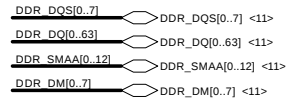
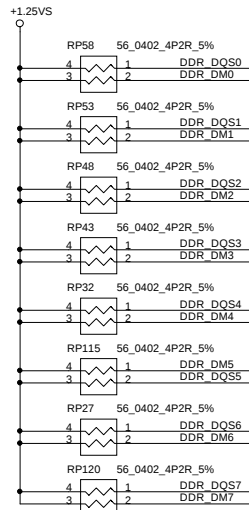
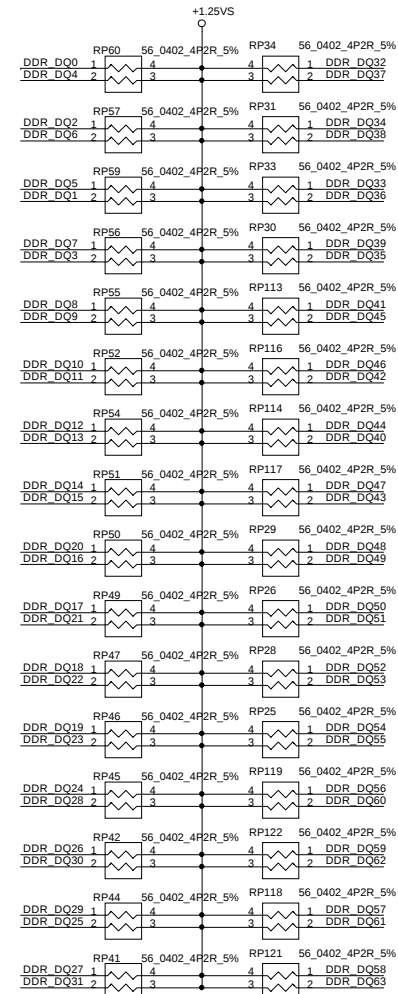


Note: Place Close to DIMM0

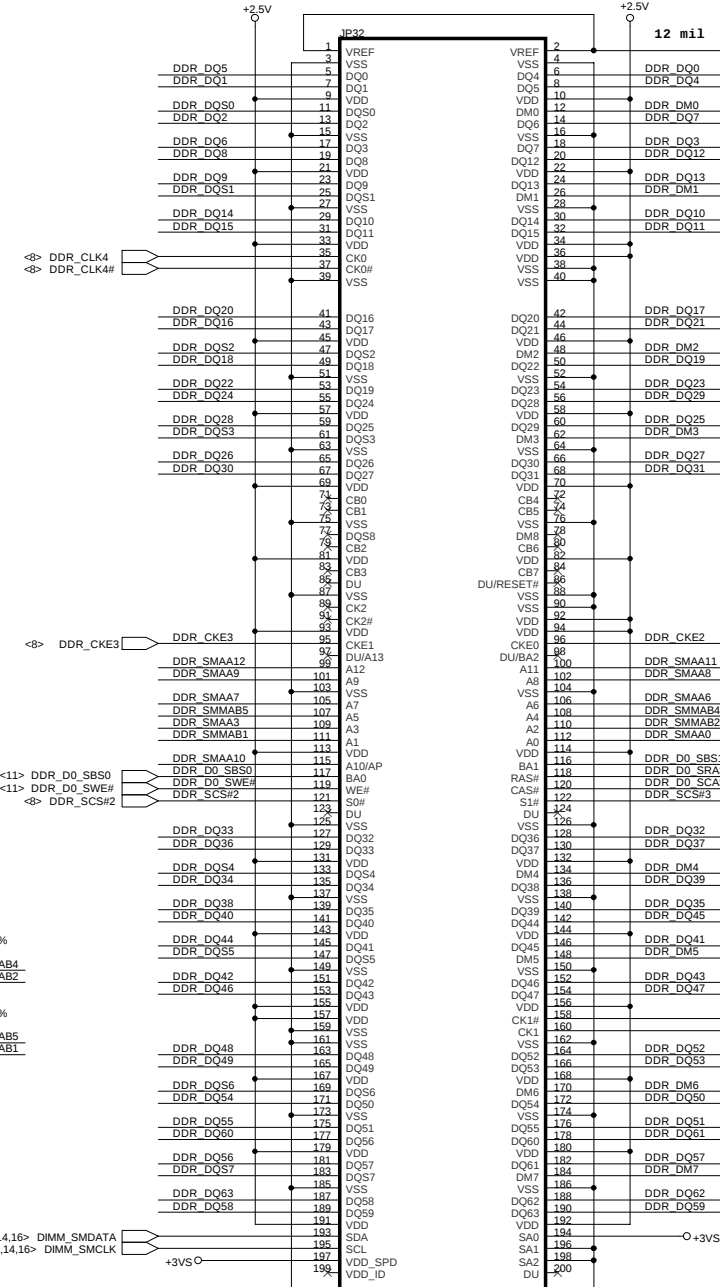


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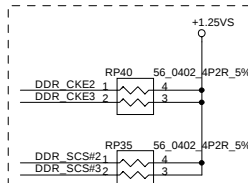
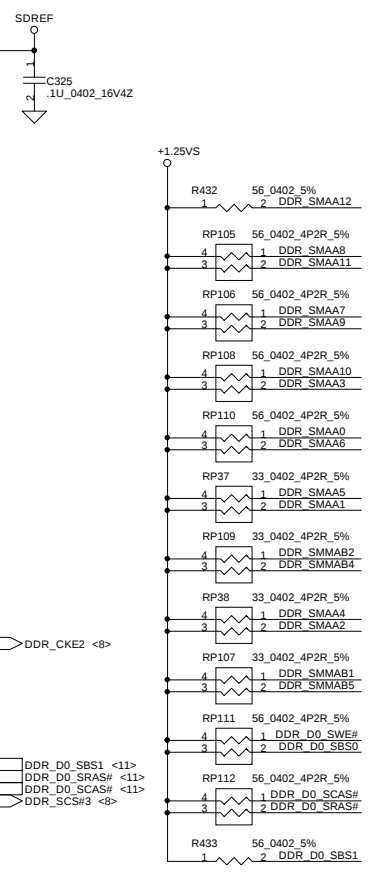
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Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil



DIMM1
Back side / H=9.2mm

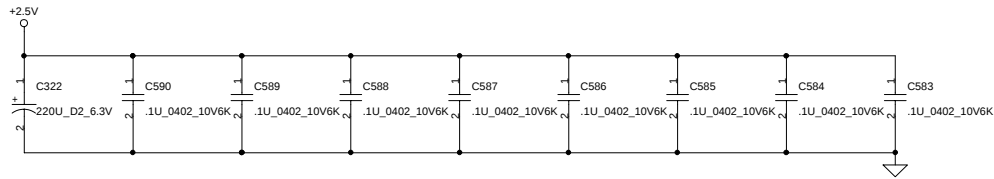


Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

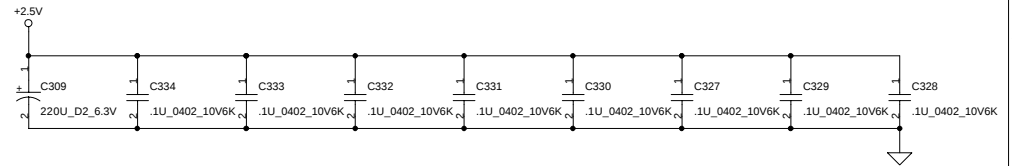
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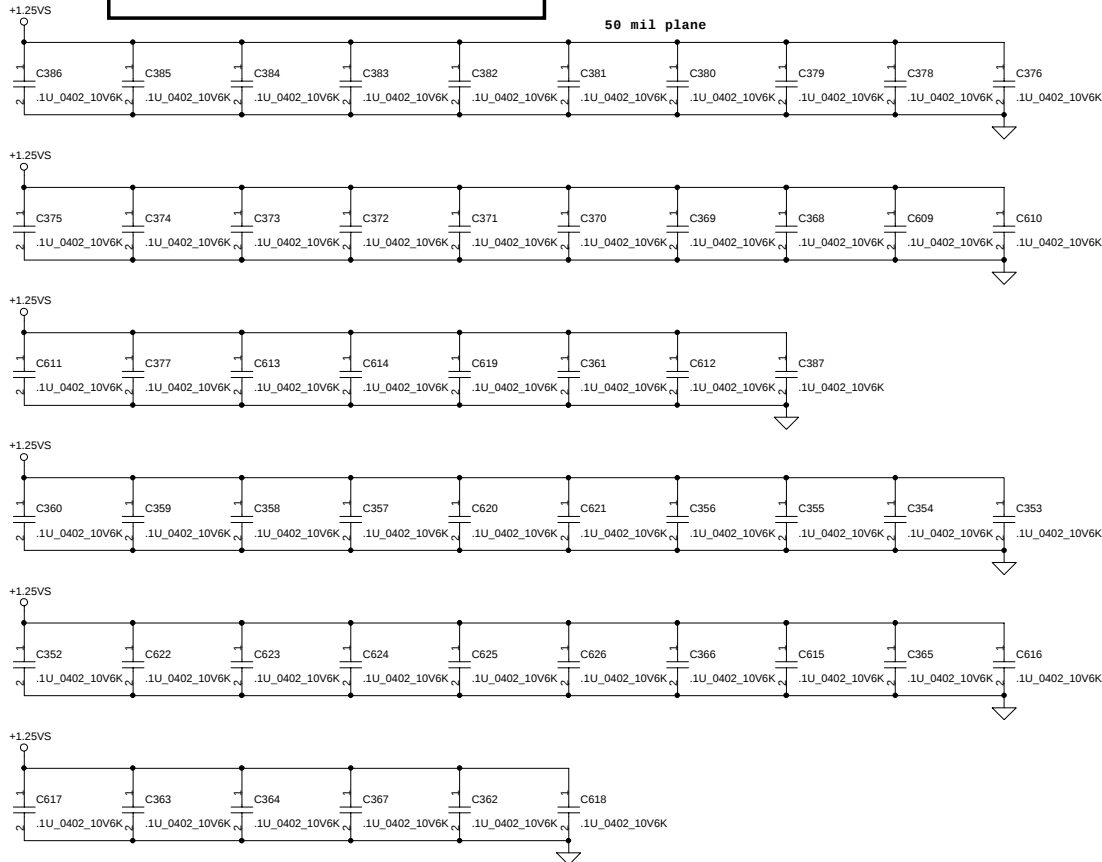
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Distribute as close as possible
to DDR-SODIMM1.



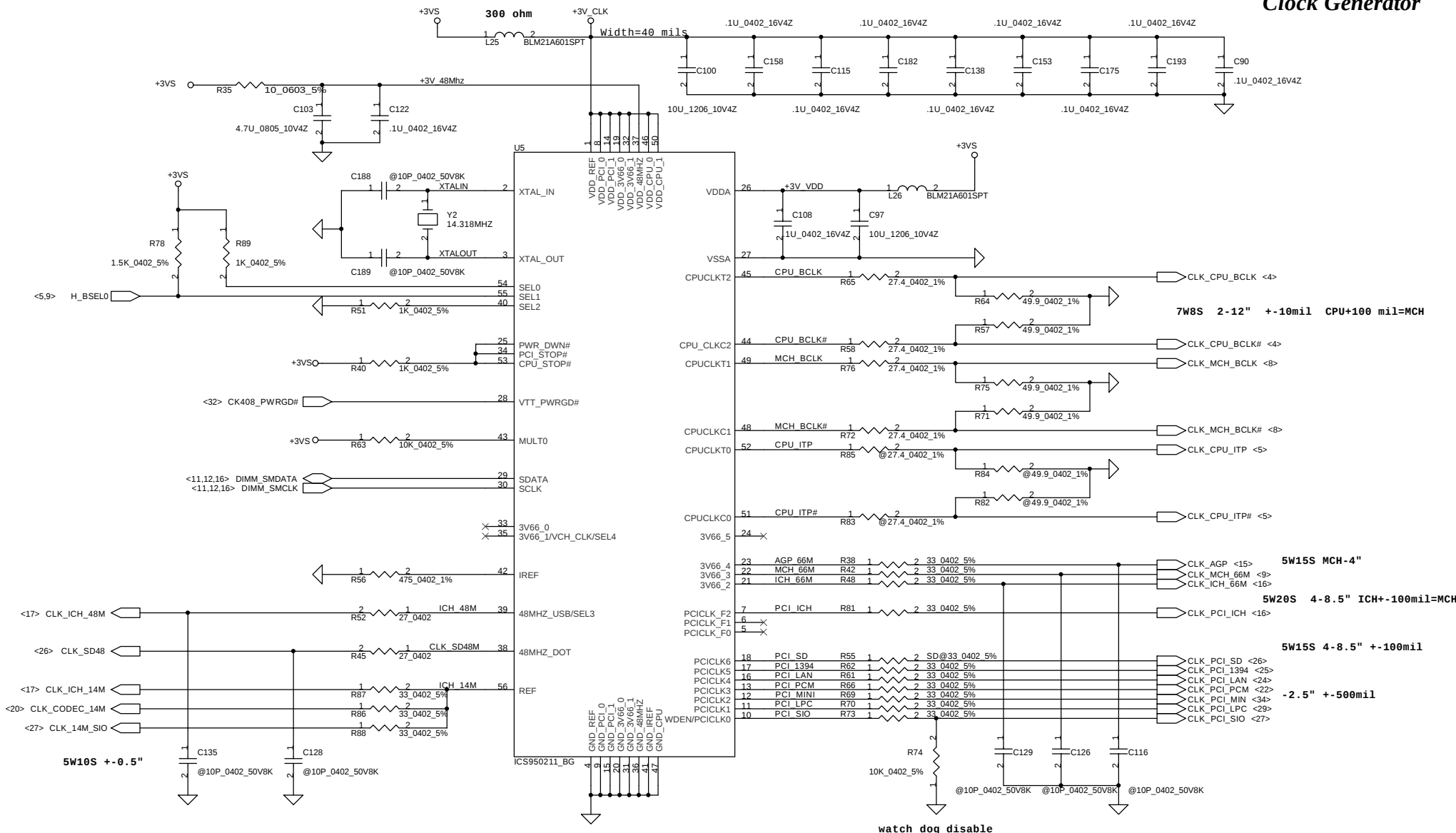
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



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Clock Generator



CPU Frequency Select Table

SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ

*

```
ground plane inside the part pads
one power plane inside the part pads
```

```
watch dog disable
```

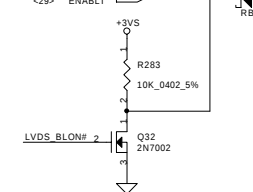
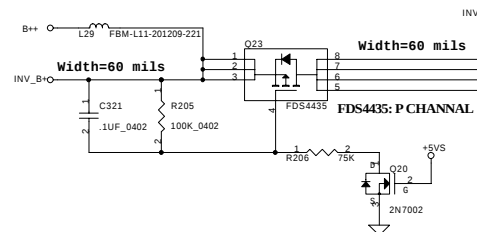
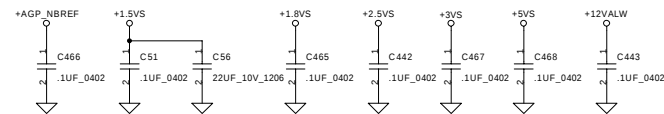
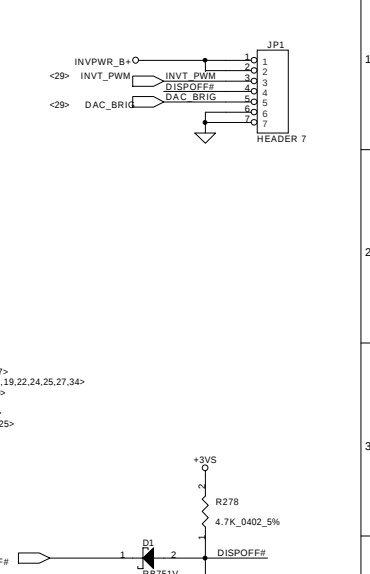
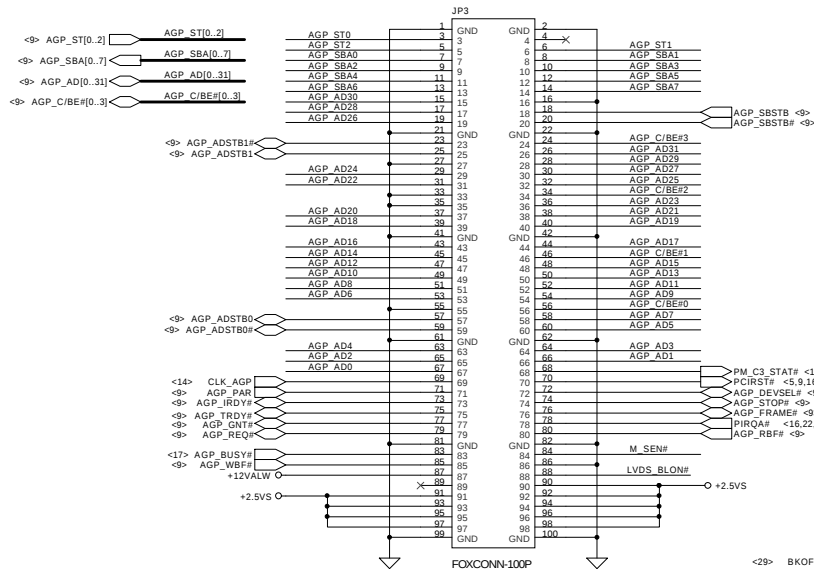
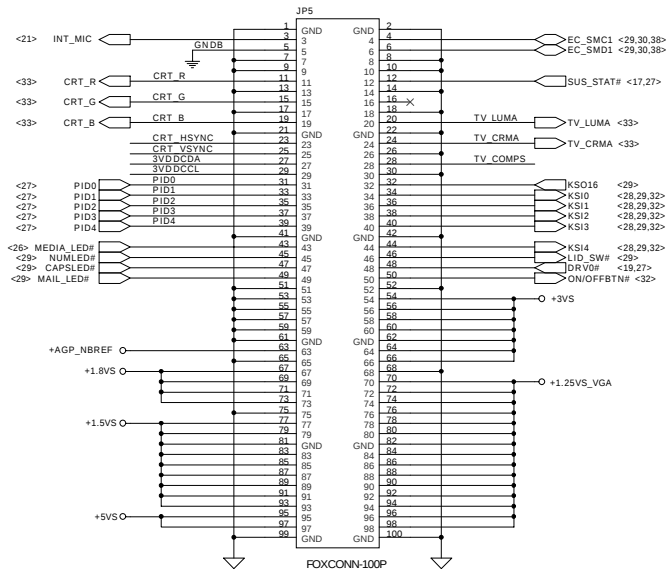
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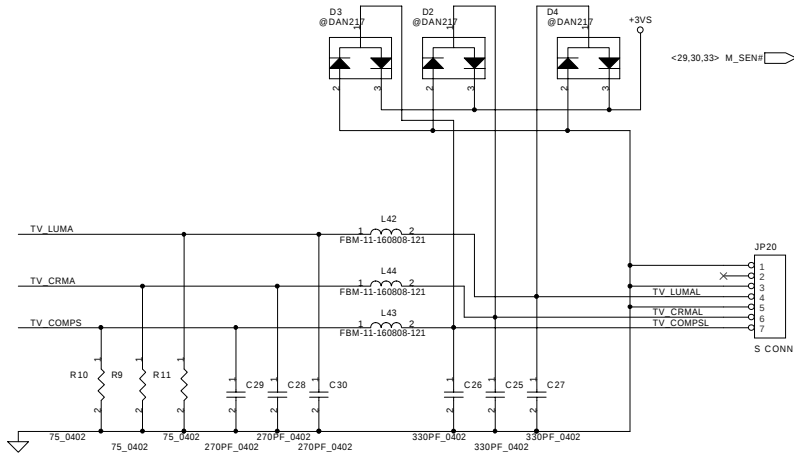
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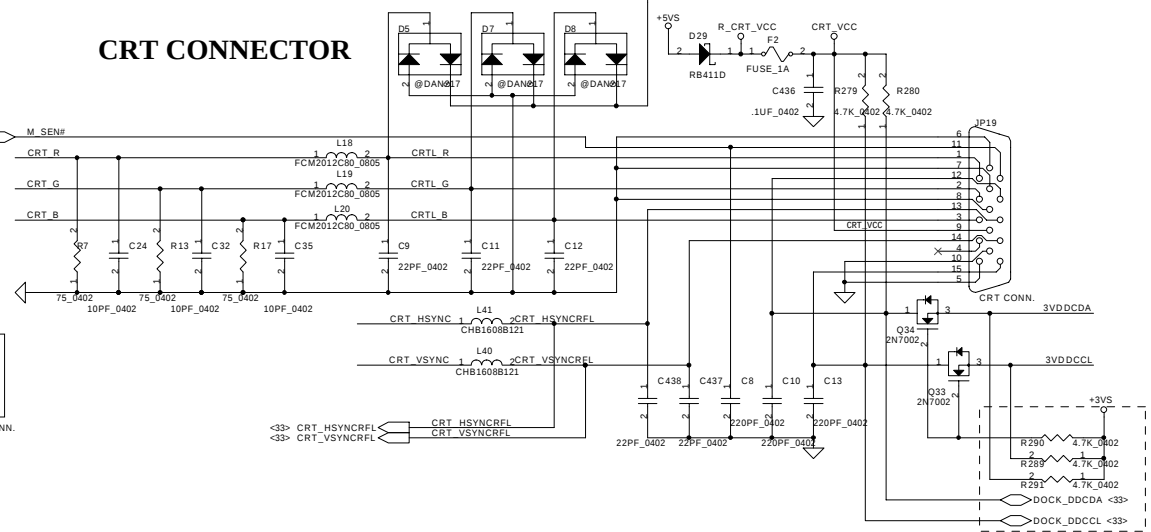
AGP 100X2 Pin connector

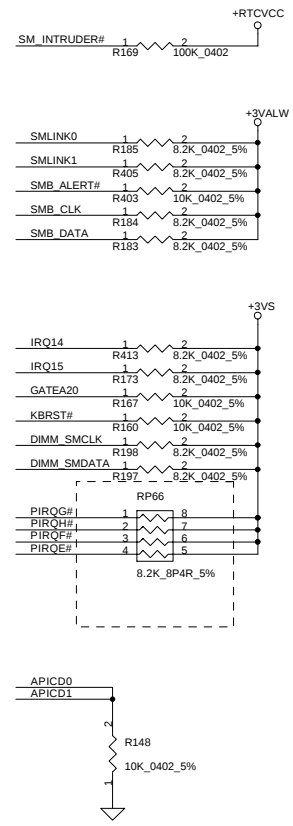
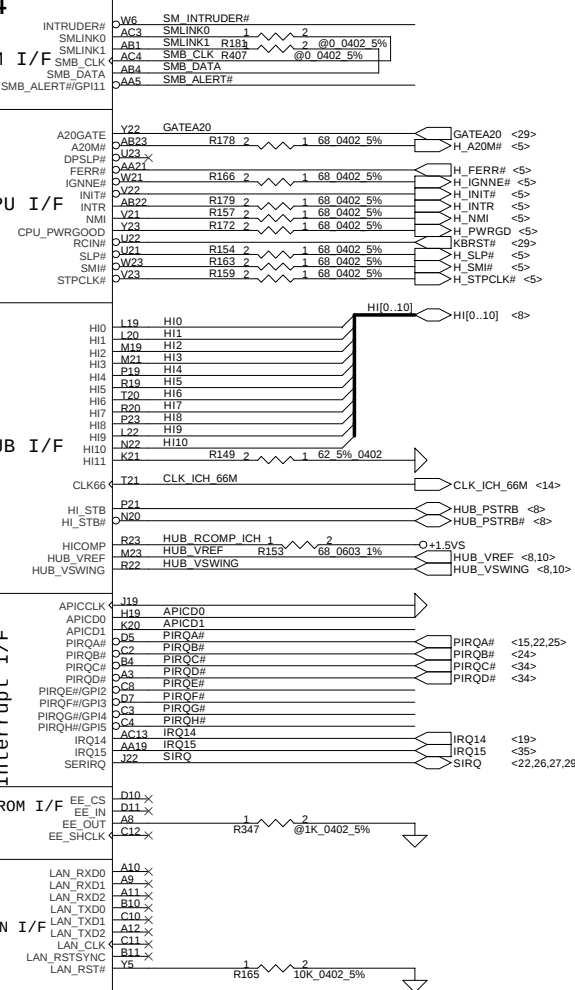
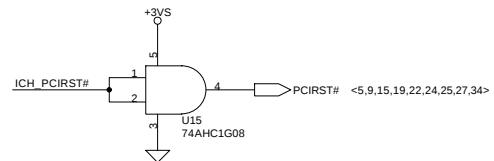
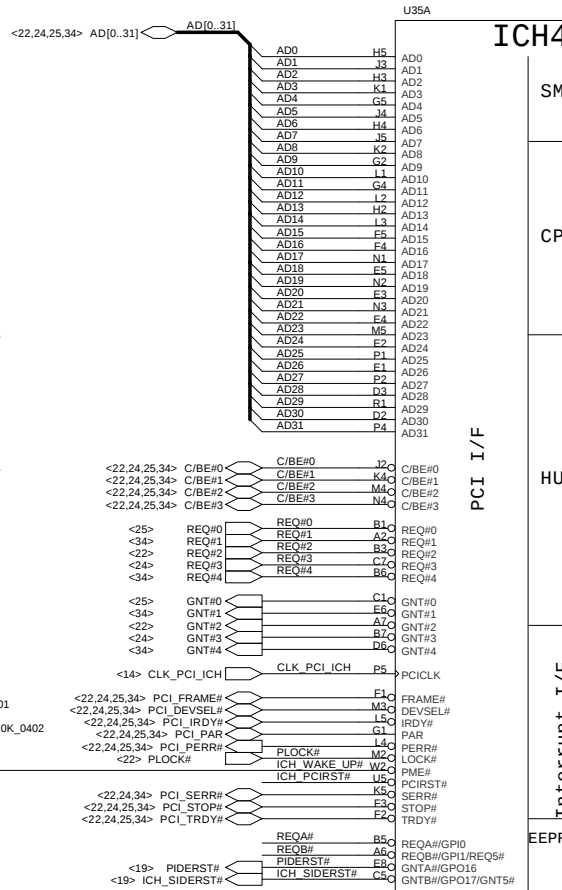
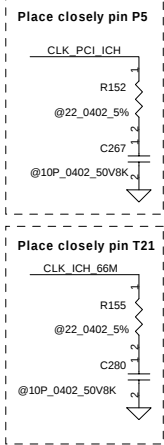
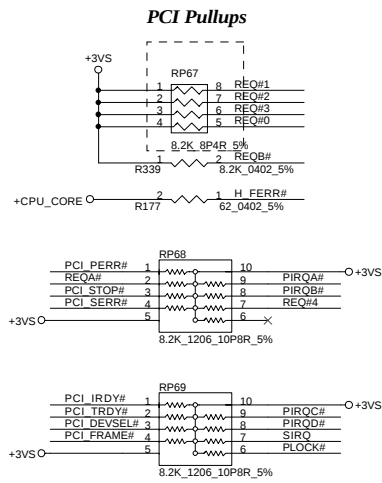


TV_OUT CONNECTOR



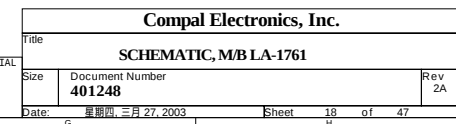
CRT CONNECTOR



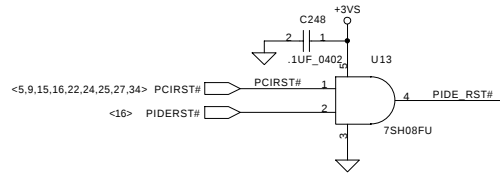


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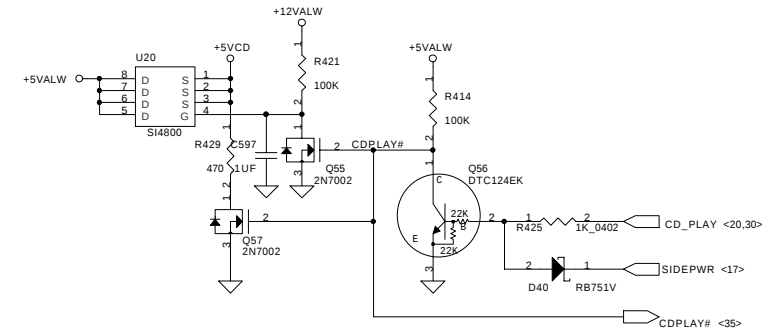
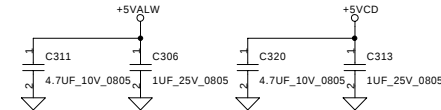
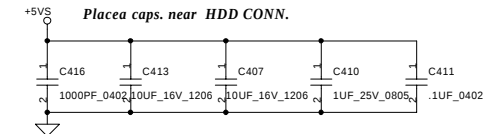
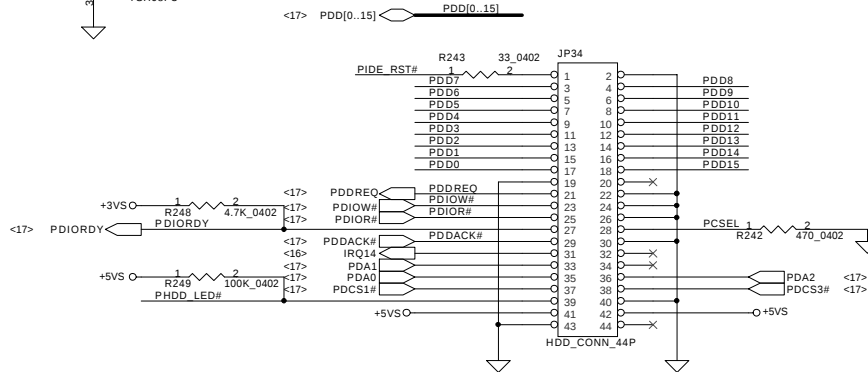
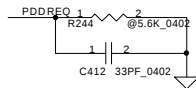
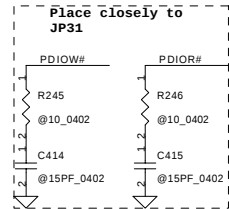
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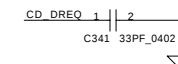
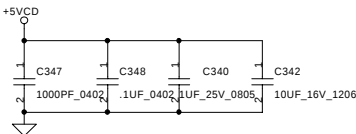
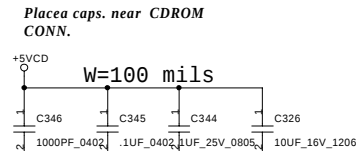
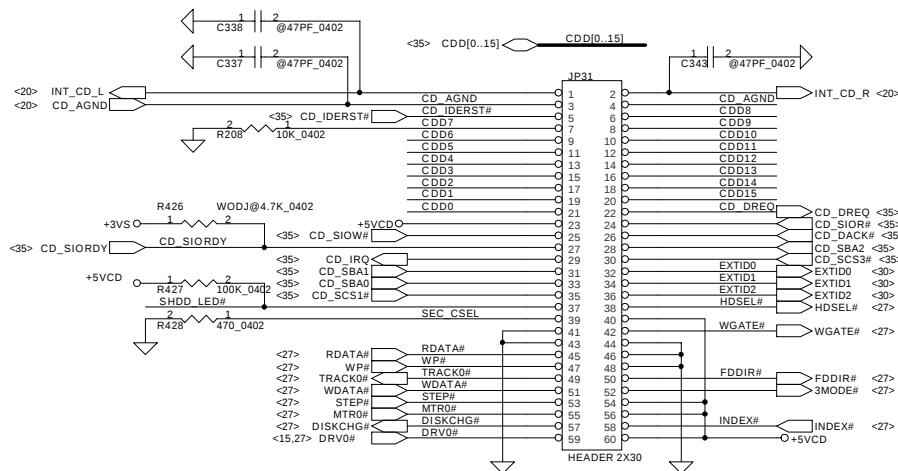
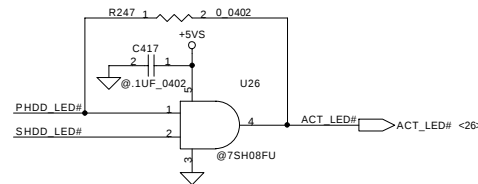
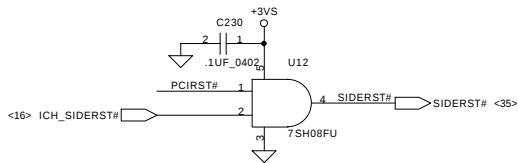
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HDD Connector



CD-ROM Connector



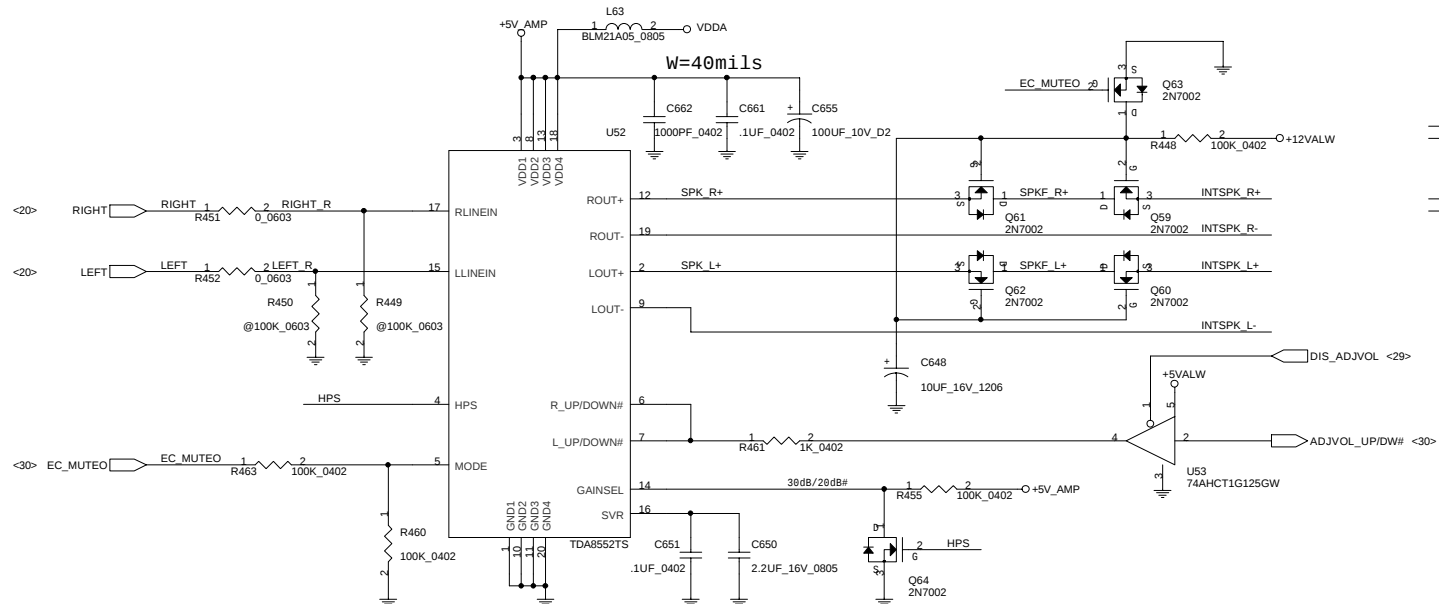
Extend Module ID list

DEVICE	EXTID2	EXTID1	EXTID0
FDD	0	0	0
CD-ROM	0	0	1
LS-120	0	1	0
2'nd HDD	0	1	1
NONE	1	1	1

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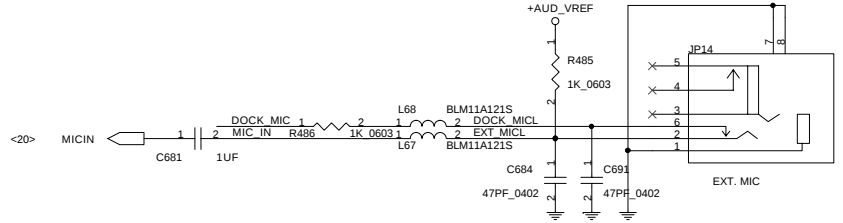
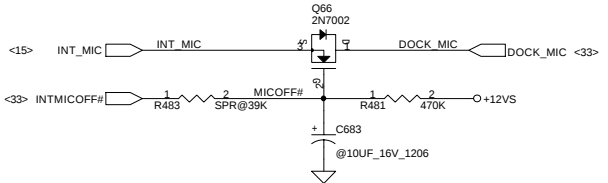
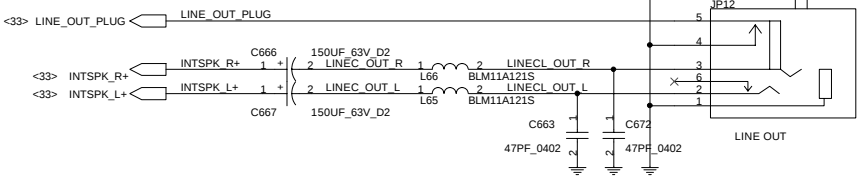
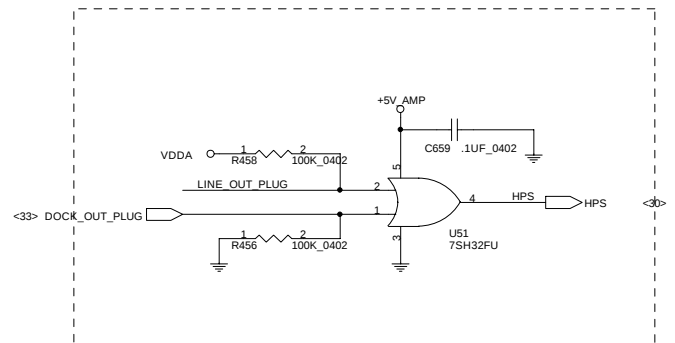
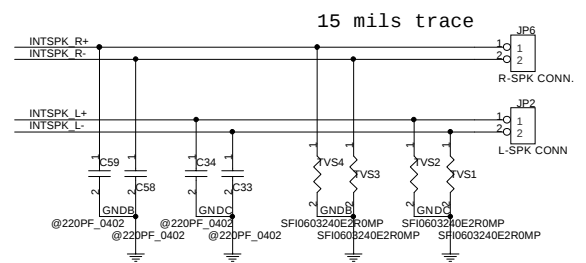
Layout note:

Trace width=15 mils.

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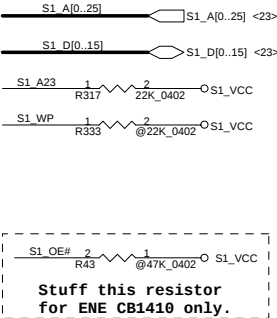
2.INTSPK_R+/- ,INTSPK_L+/-

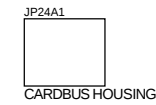
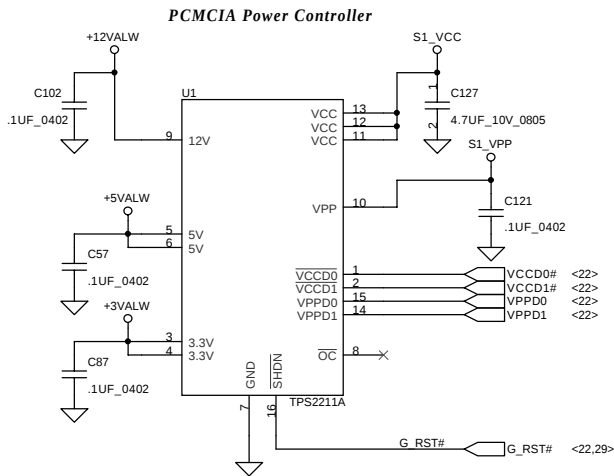
3.LINEOUT_L, LINEOUT_R



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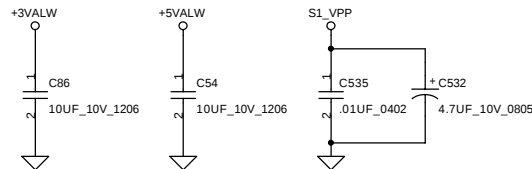
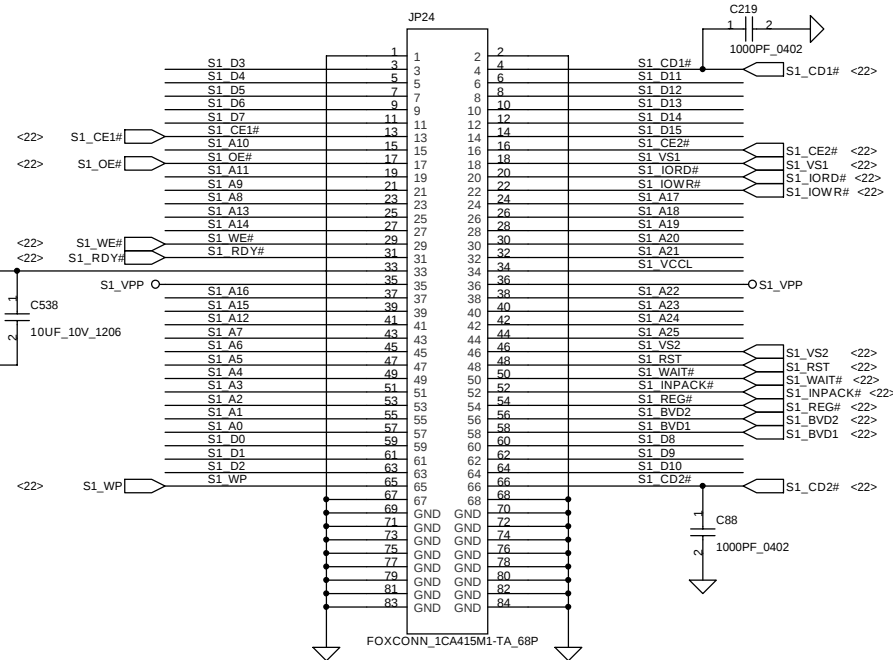
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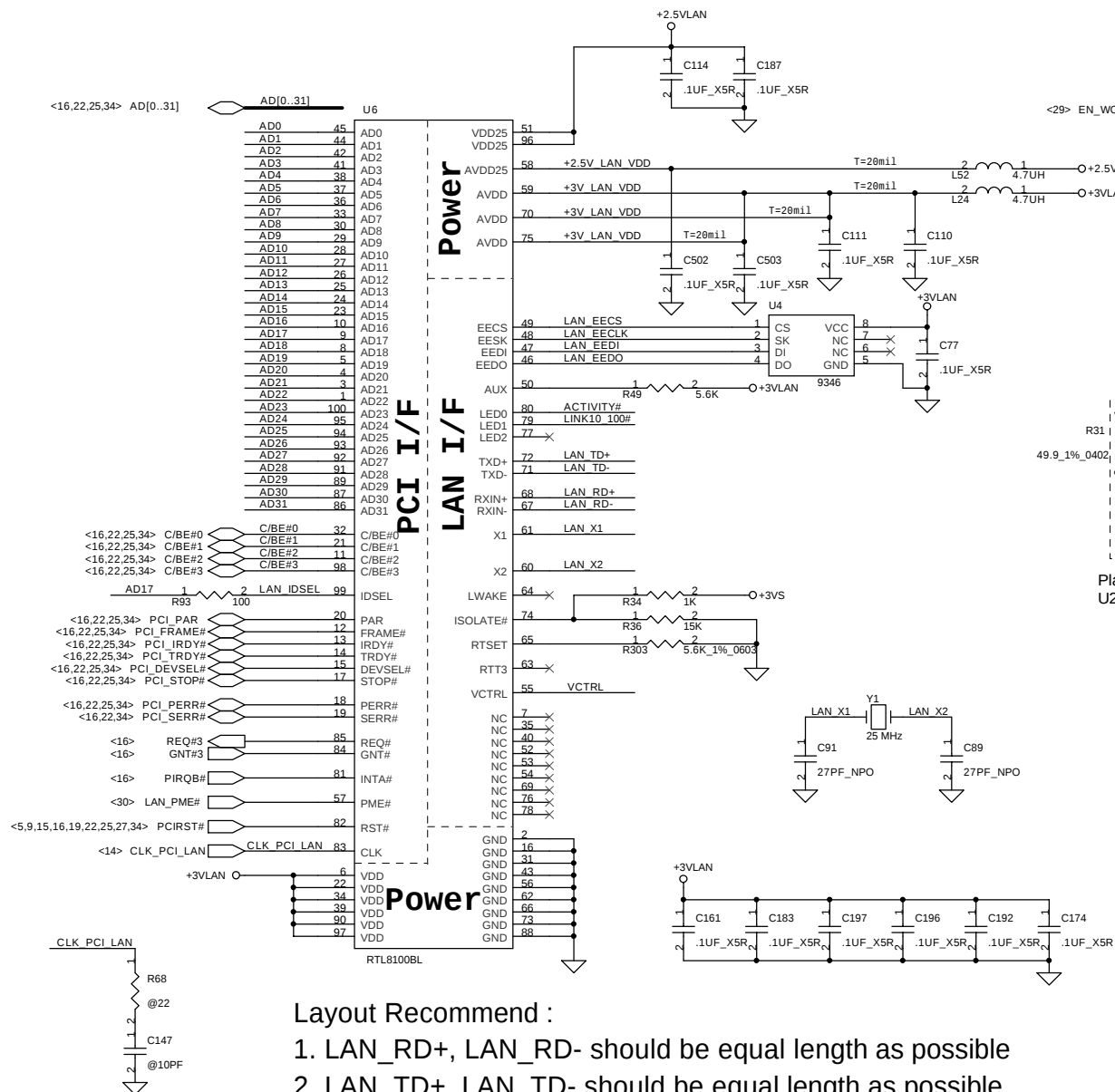
CardBus Socket

<22> S1_A[0..25] S1_A[0..25]
<22> S1_D[0..15] S1_D[0..15]



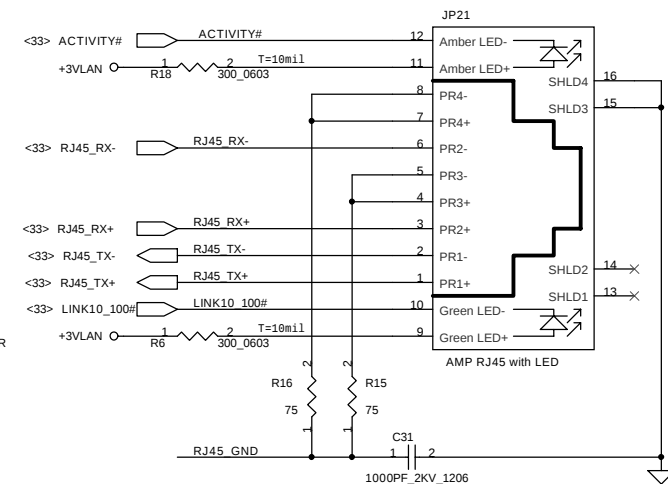
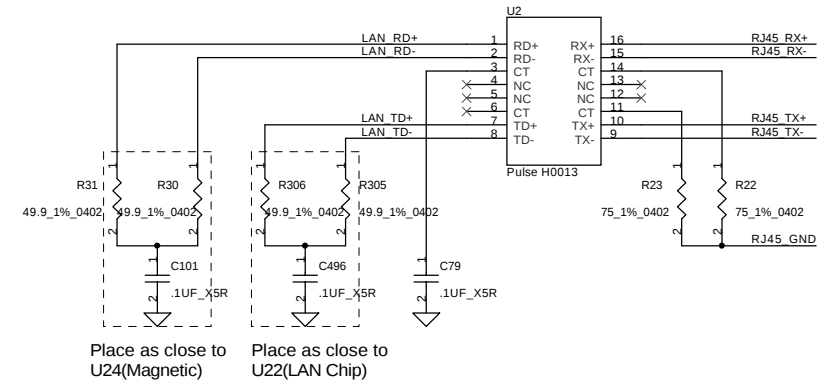
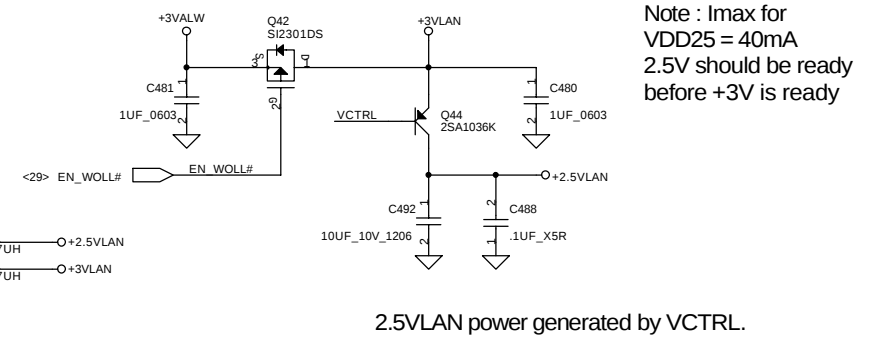
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Layout Recommend :

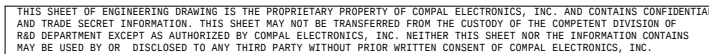
1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible



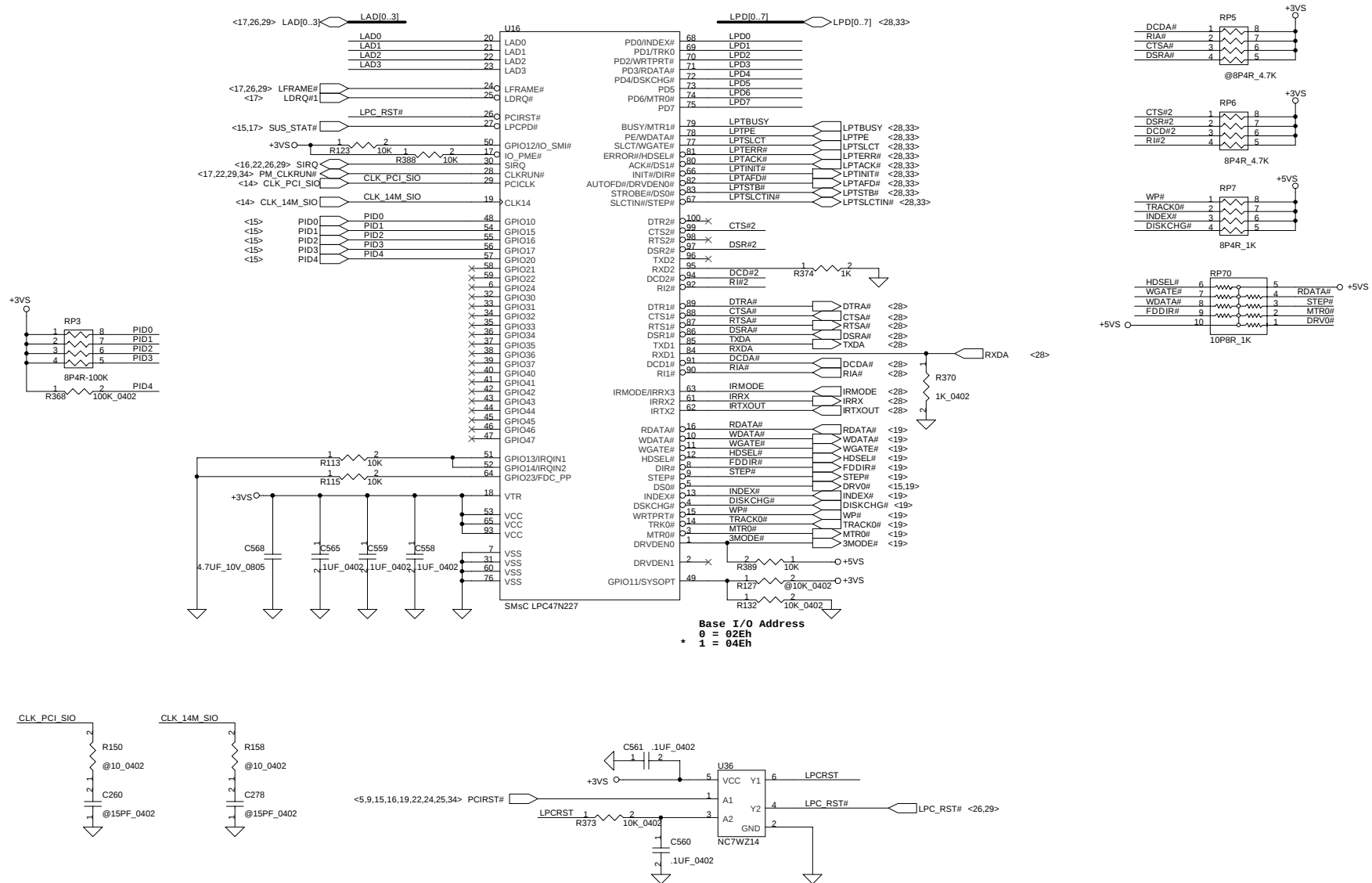
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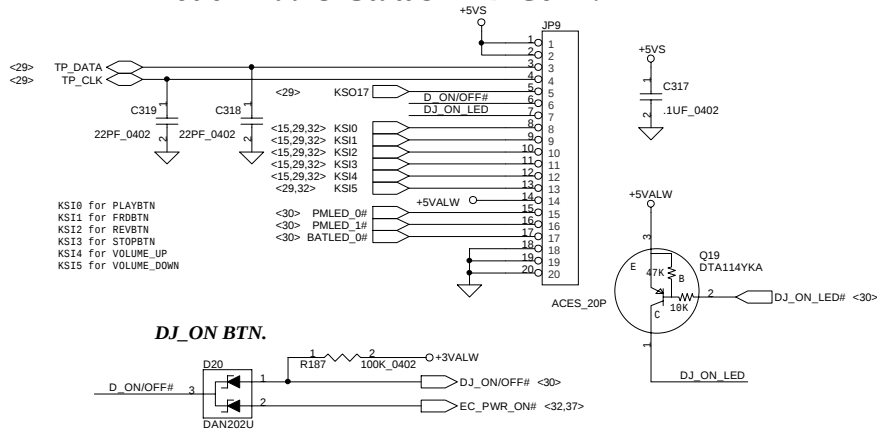
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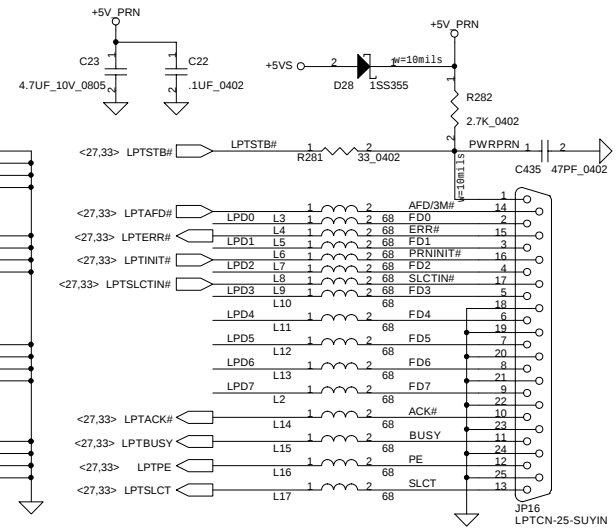
SUPER I/O SMsC FDC47N227



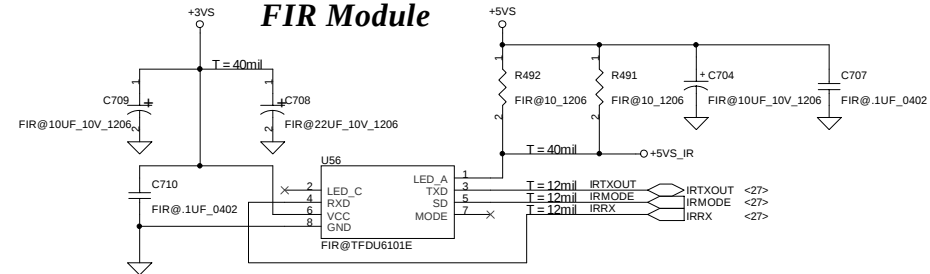
Touch Pad & Status LED Conn.



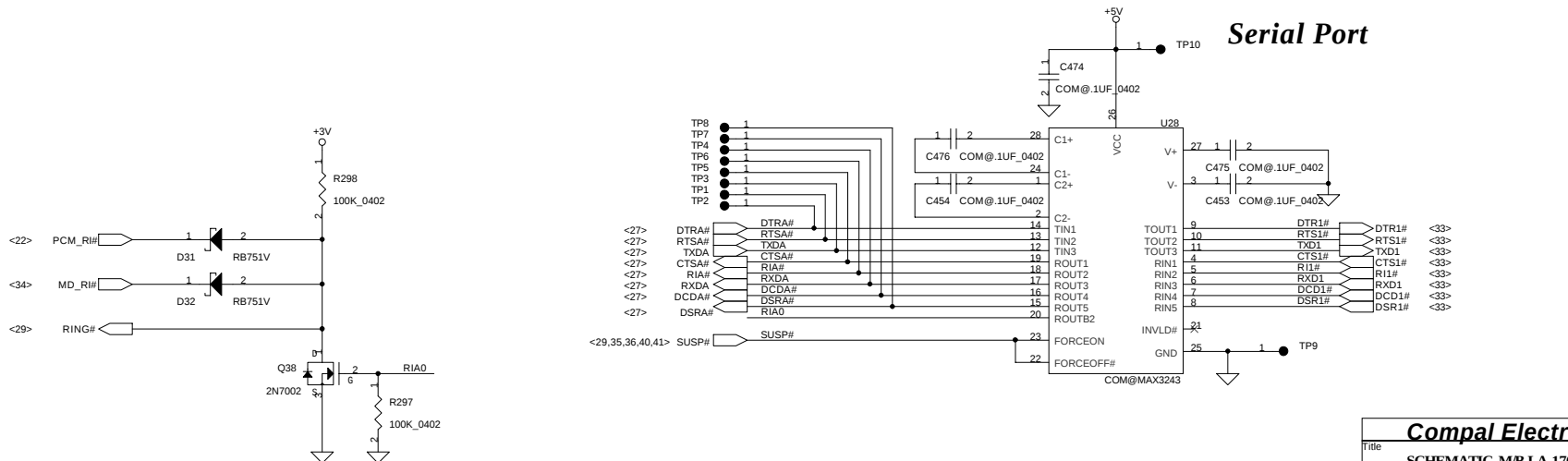
Parallel Port



FIR Module



Serial Port

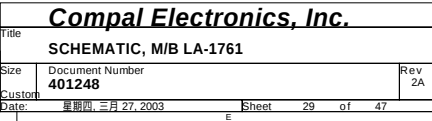


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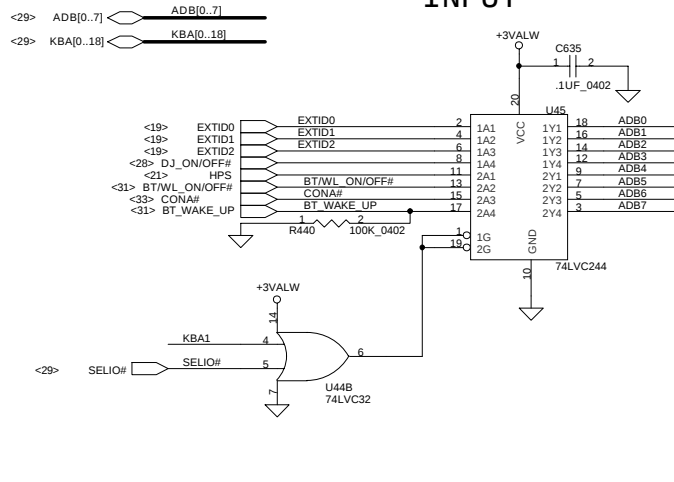
Compal Electronics, Inc.

SCHEMATIC, MB LA-1761

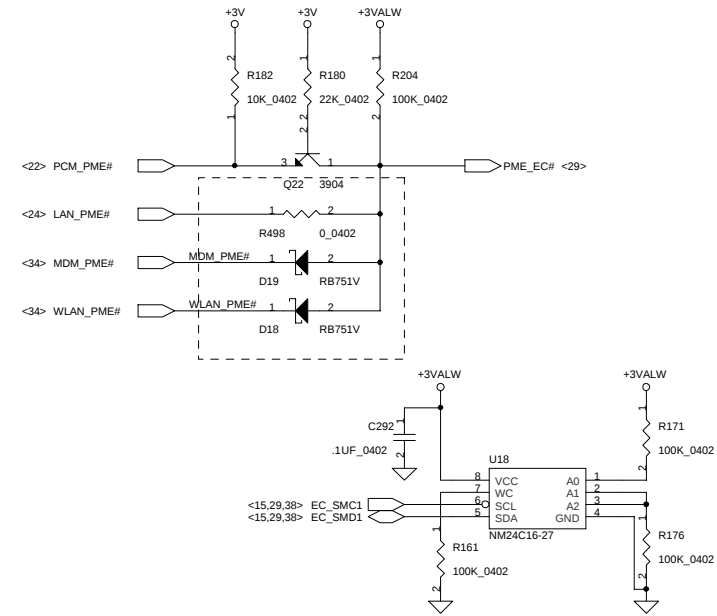
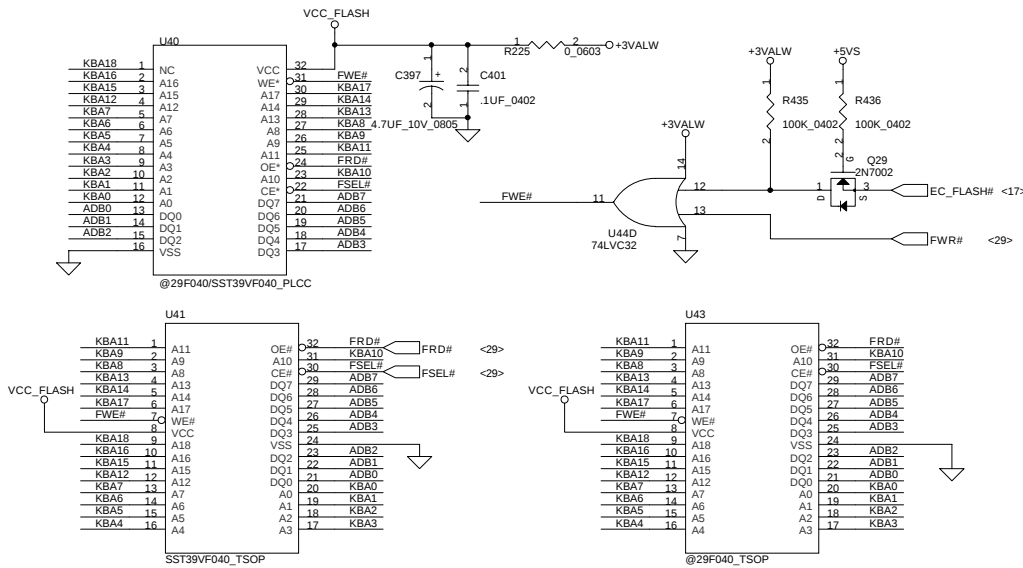
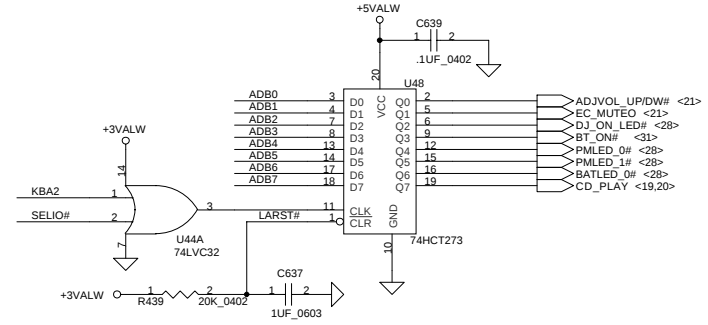
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INPUT



OUTPUT



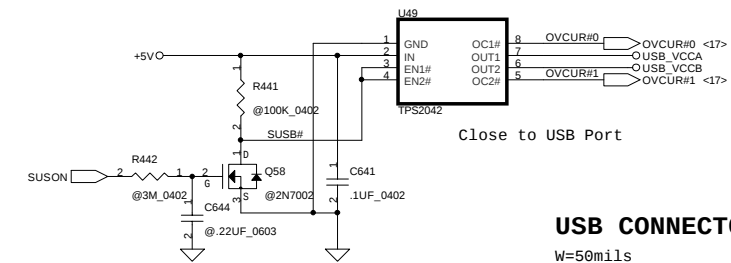
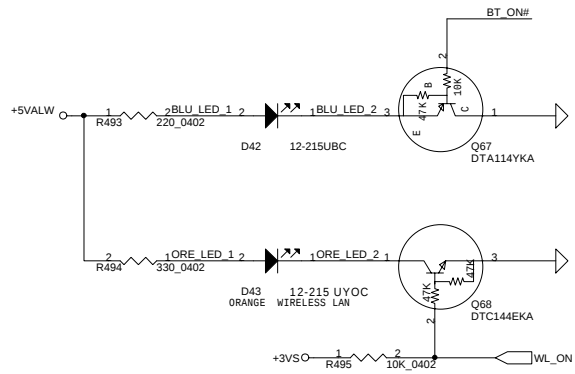
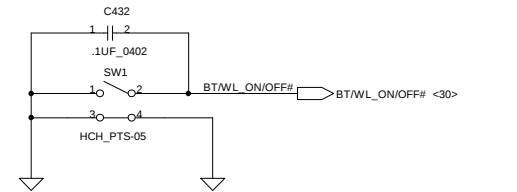
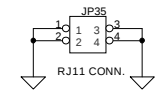
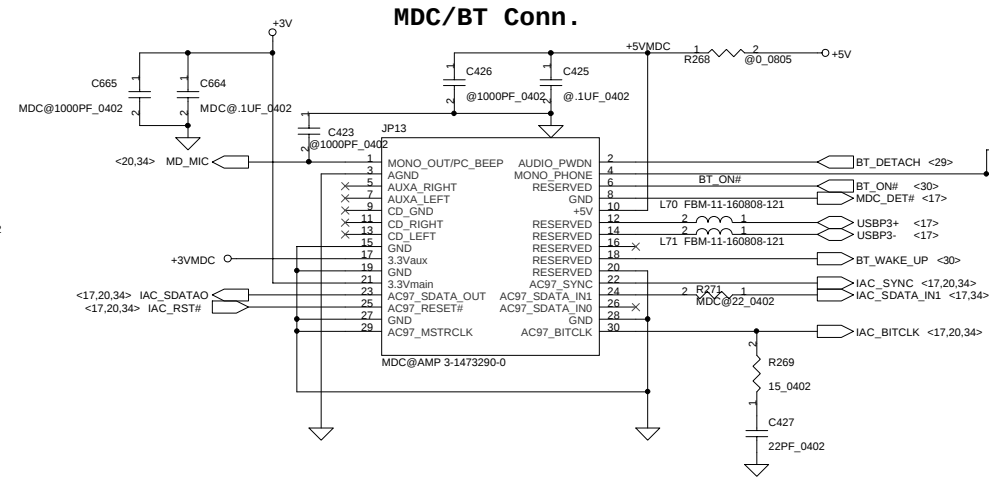
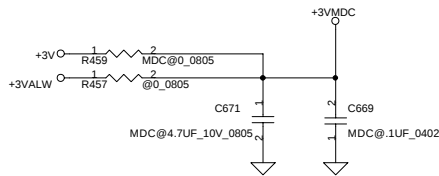
TSOP 8x14

TSOP 8x20

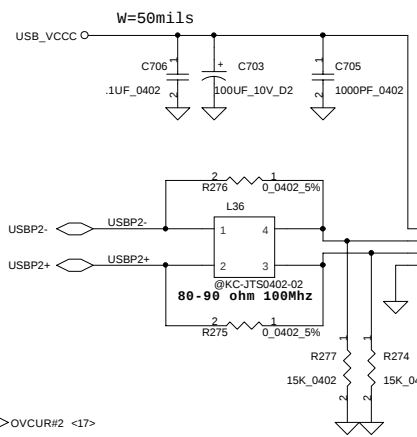
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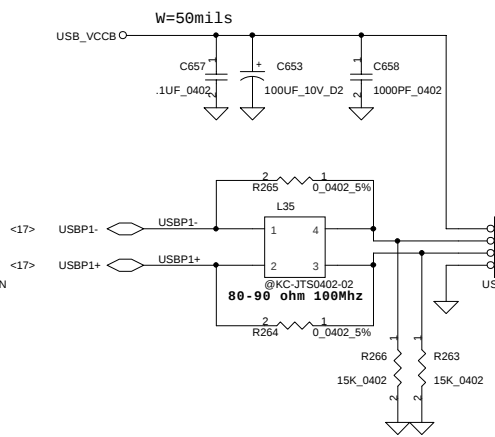
MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem



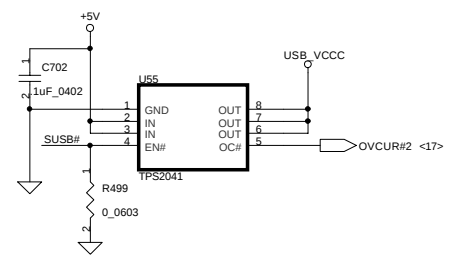
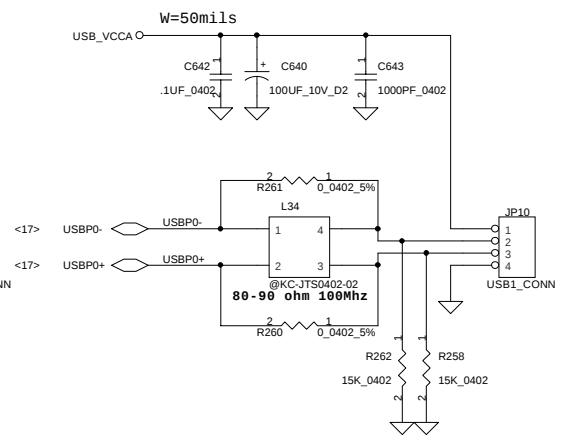
USB CONNECTOR 3



USB CONNECTOR 2



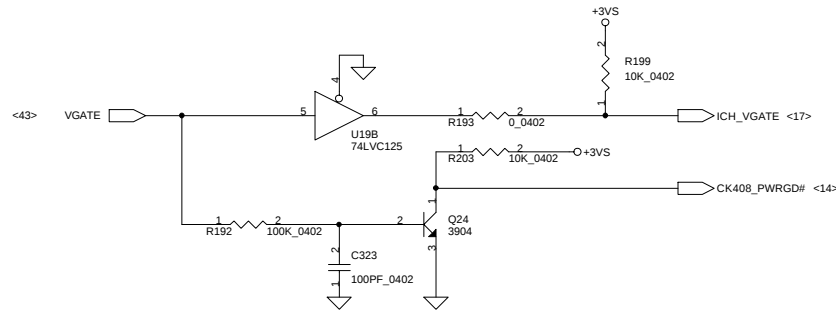
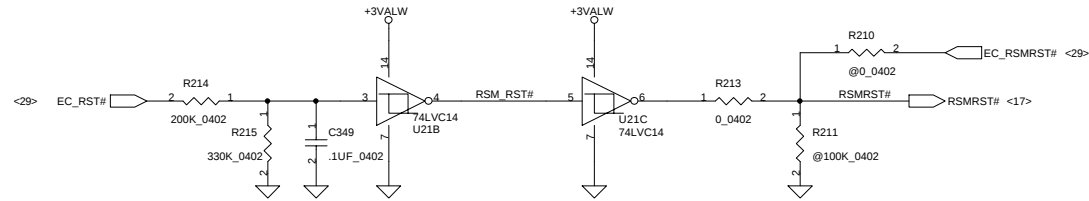
USB CONNECTOR 1



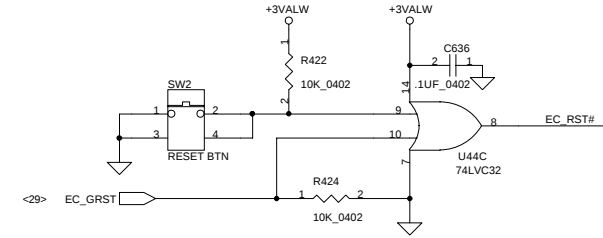
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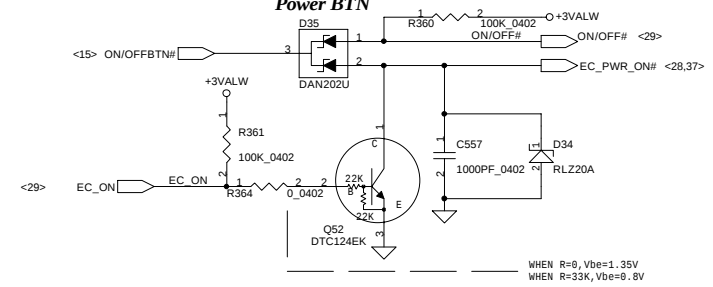
Power ON Circuit



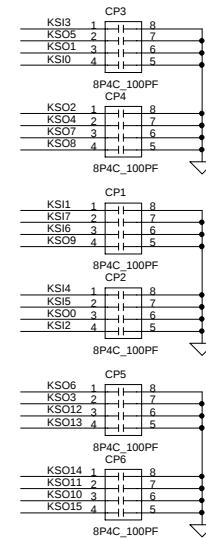
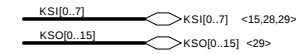
Reset Button



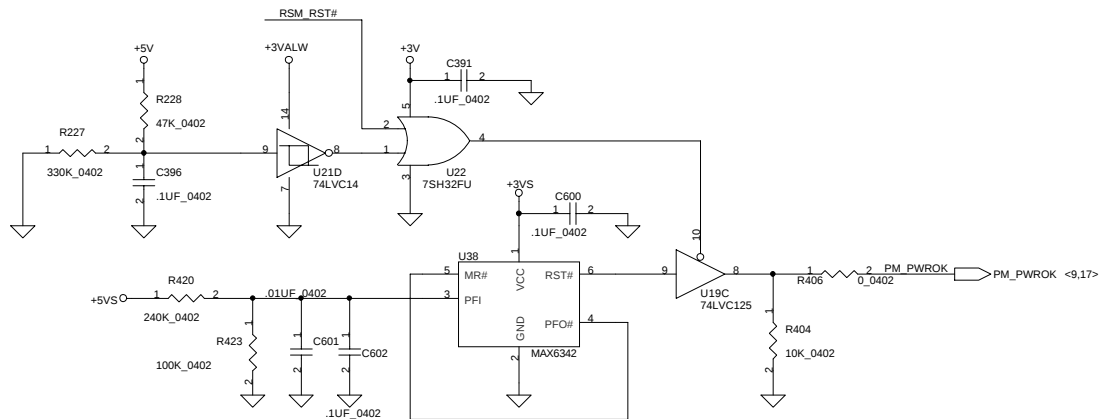
Power BTN



INT_KBD CONN.



DT : INSTALL

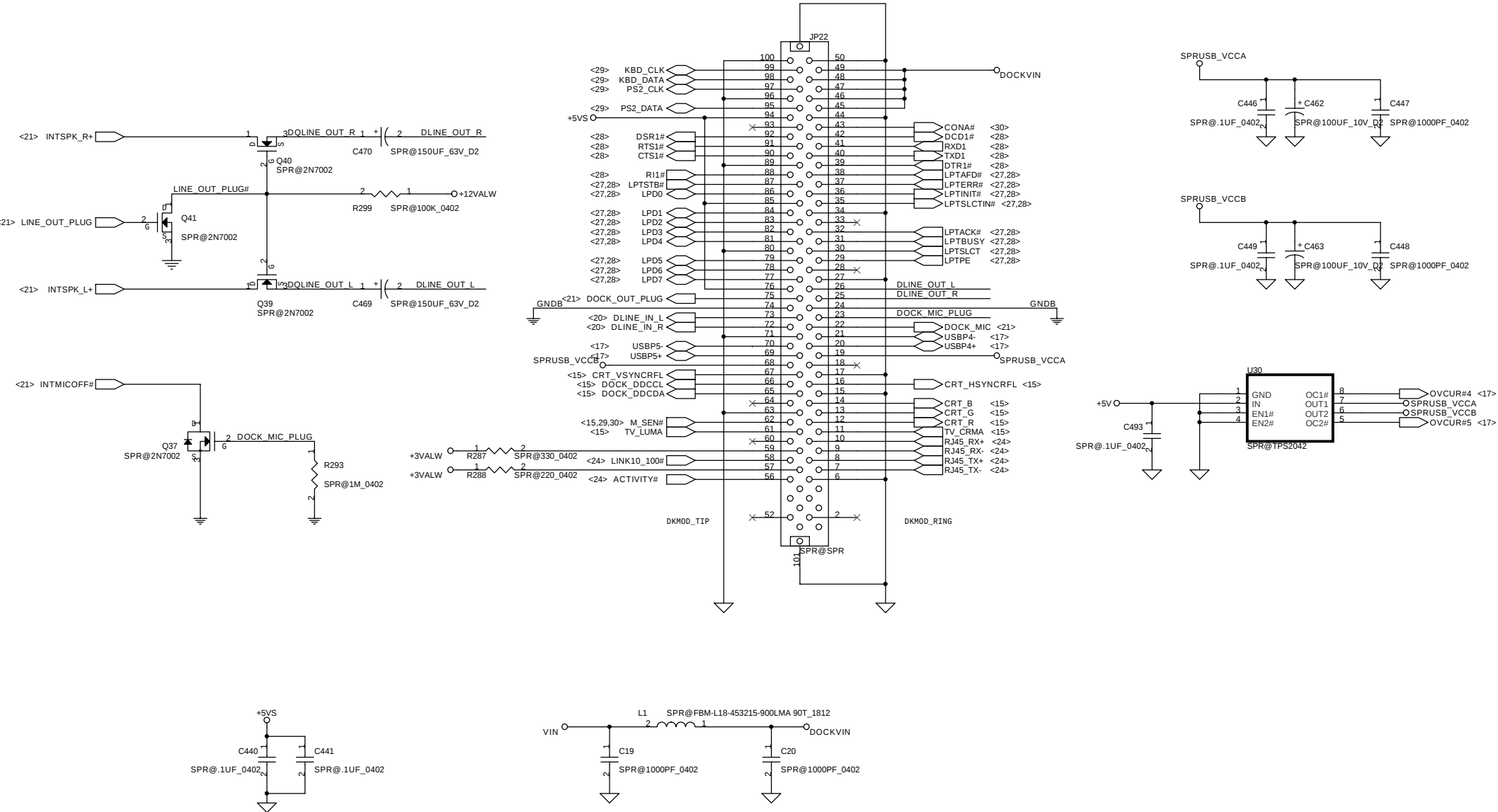


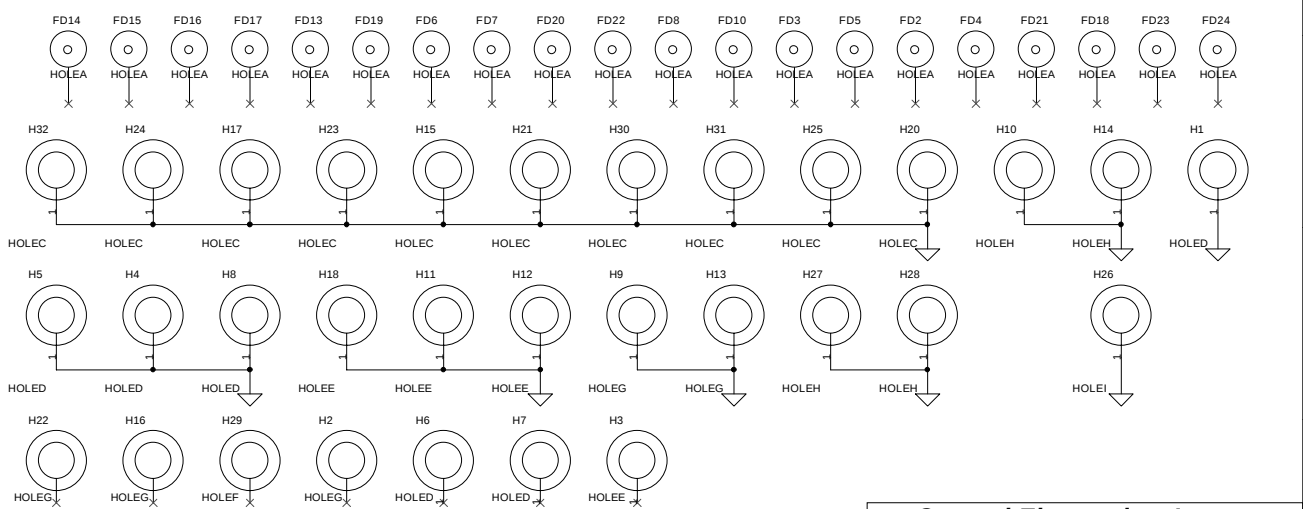
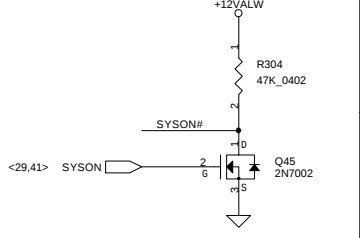
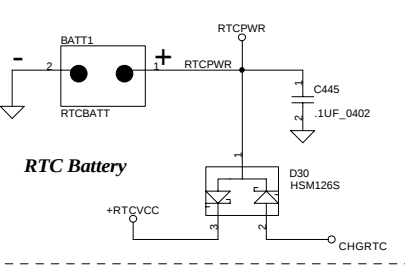
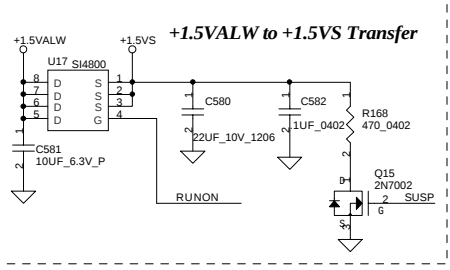
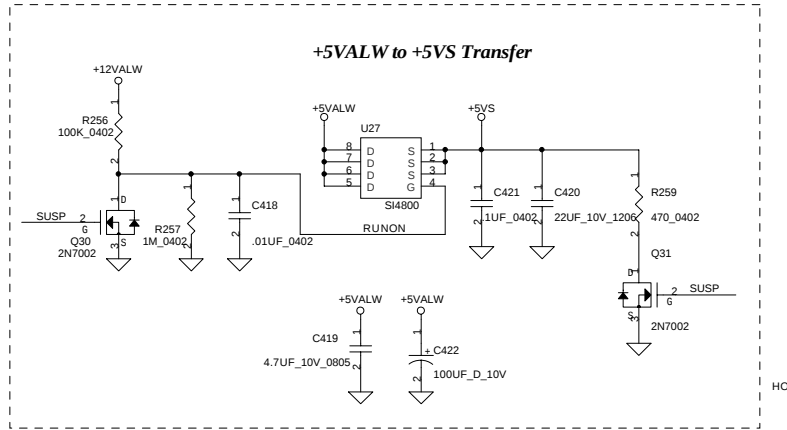
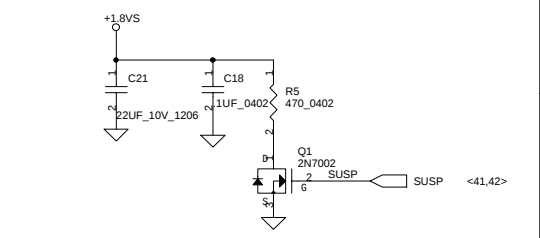
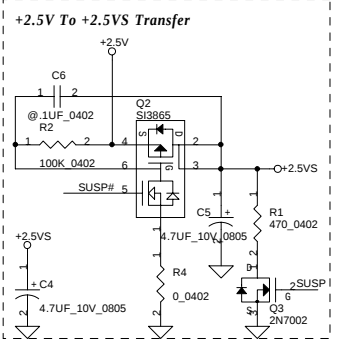
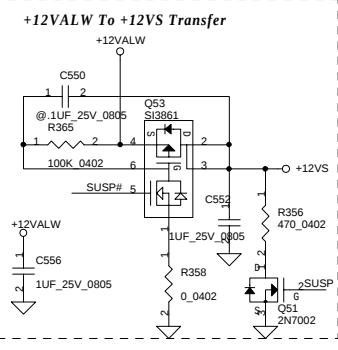
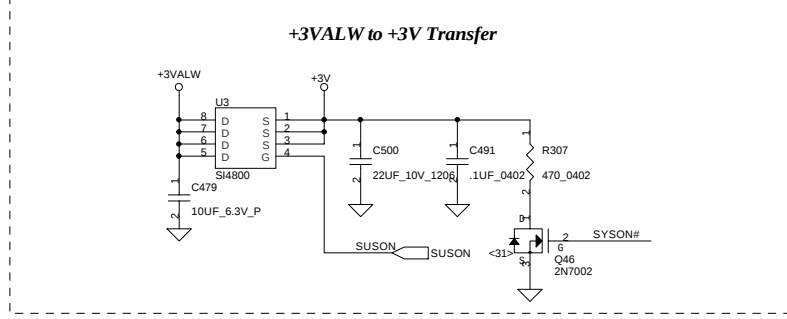
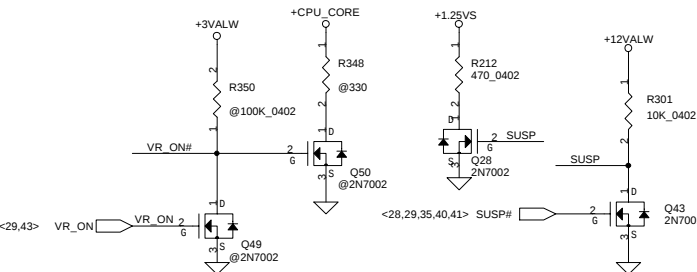
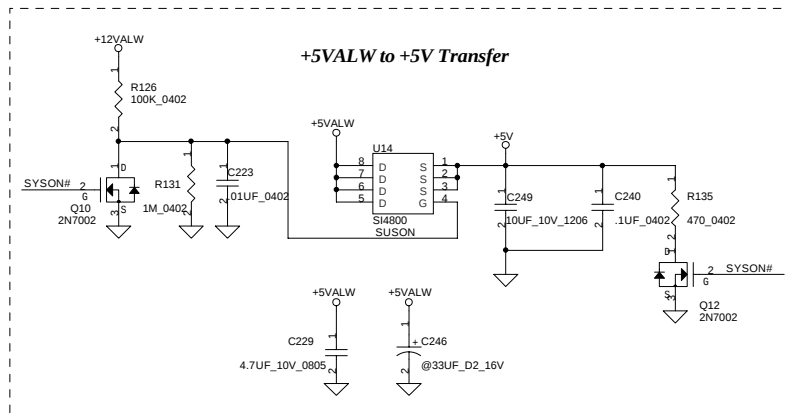
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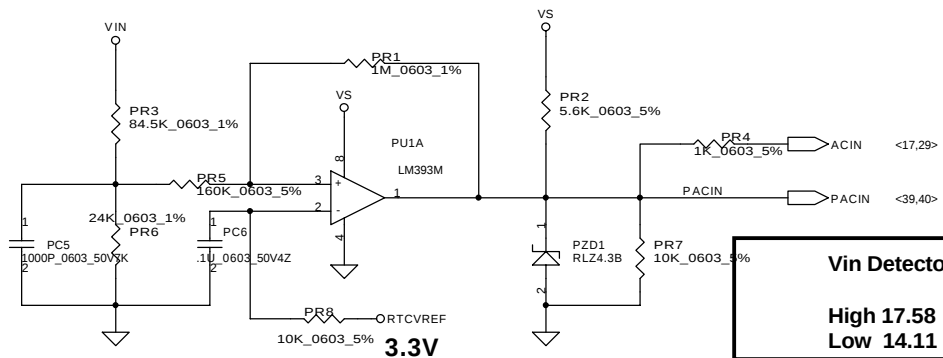
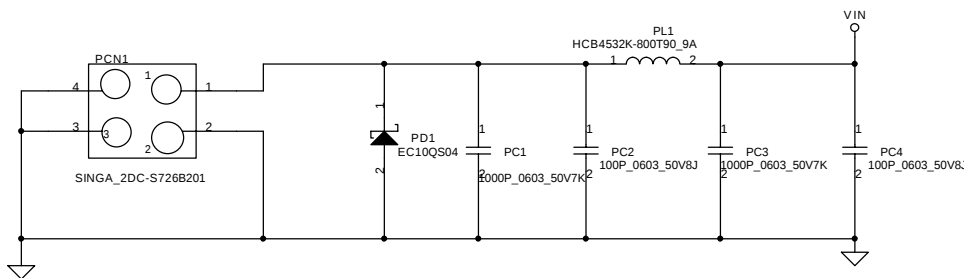
SPR 102 PIN



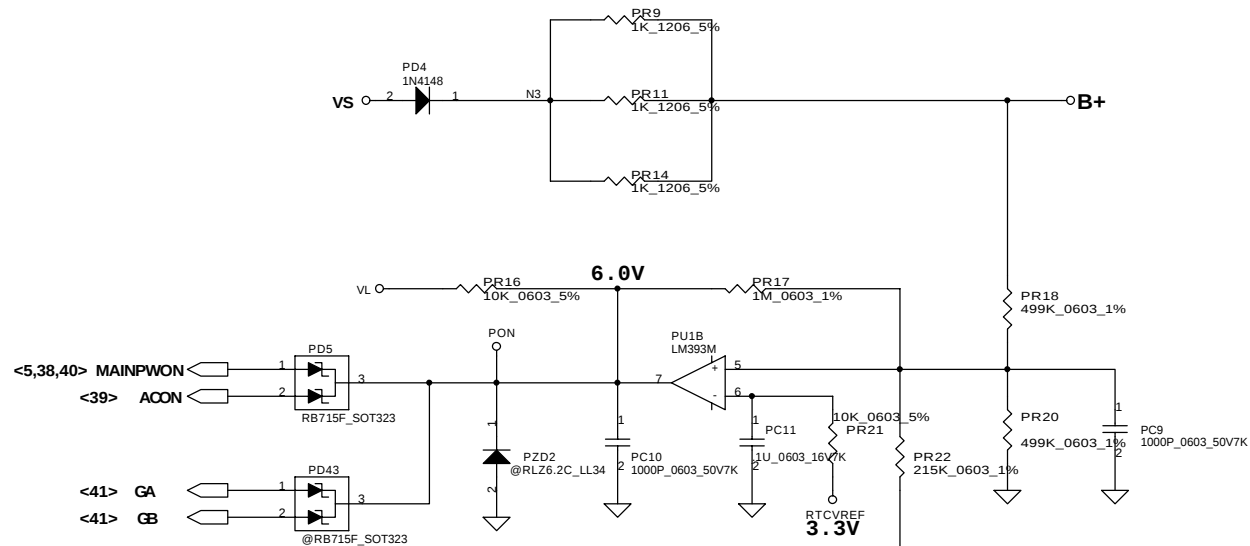
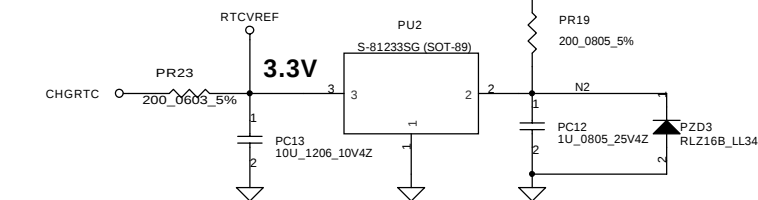
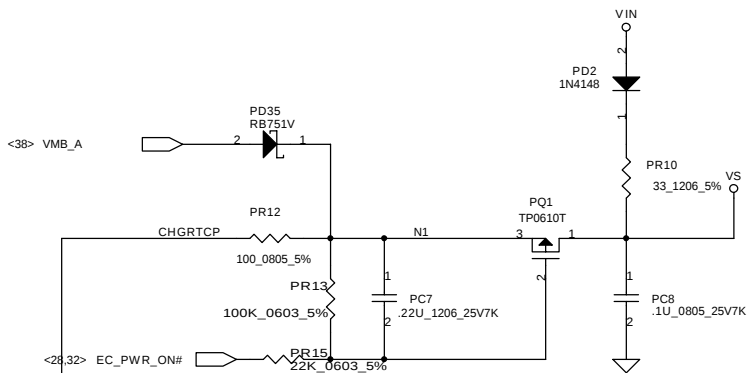


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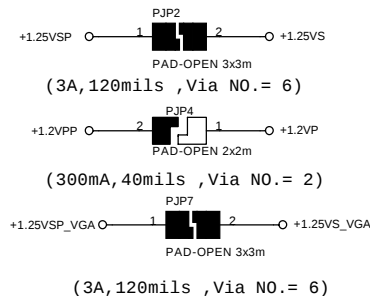
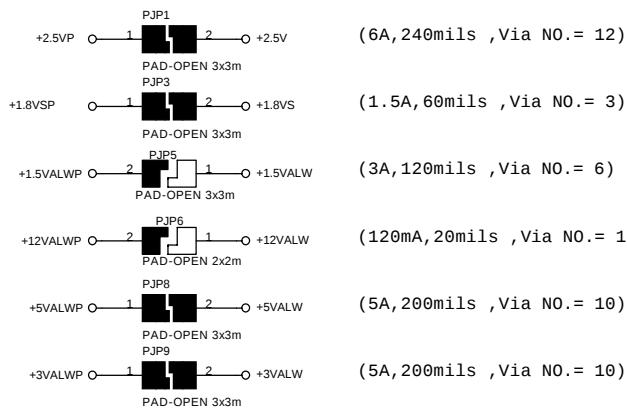
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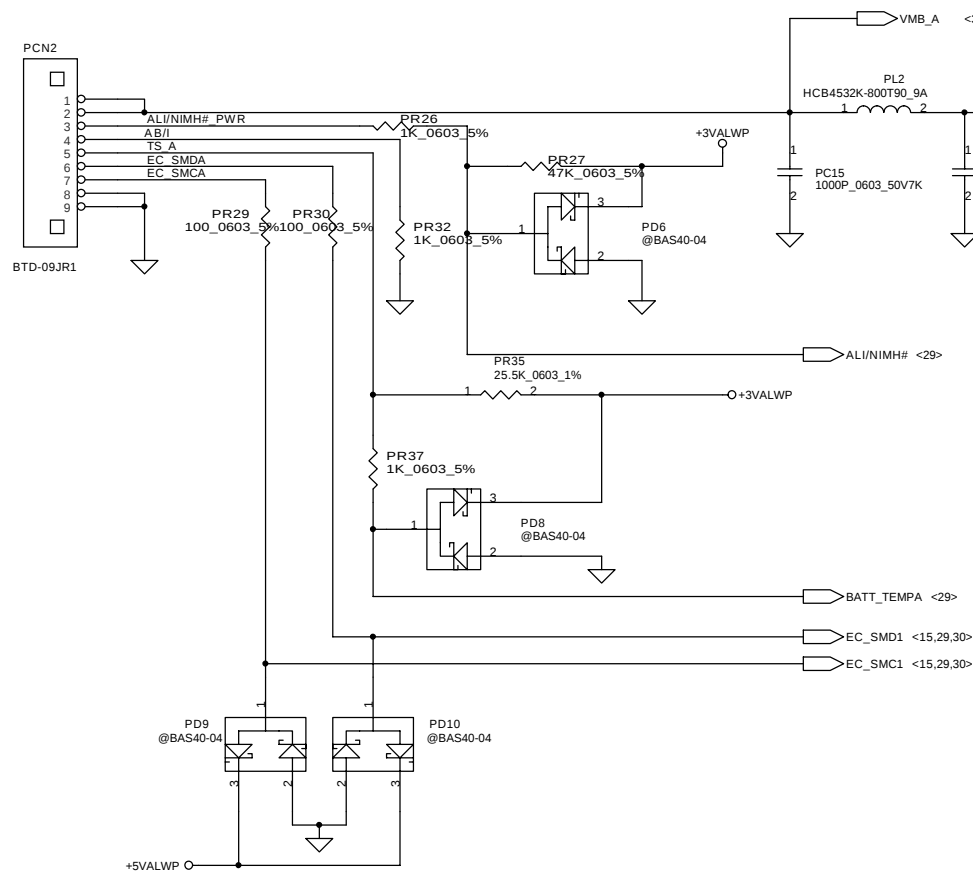
Vin Detector
High 17.58
Low 14.11



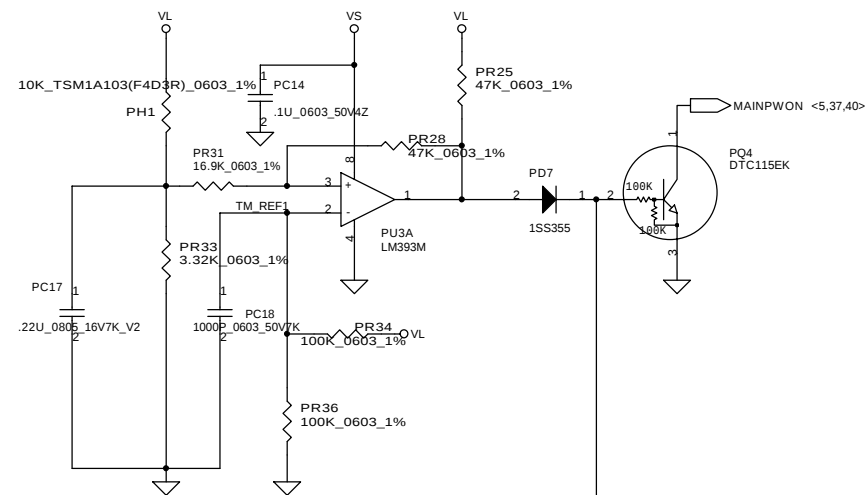
ACIN Precharge detector
15.34 15.90 16.48
13.13 13.71 14.20



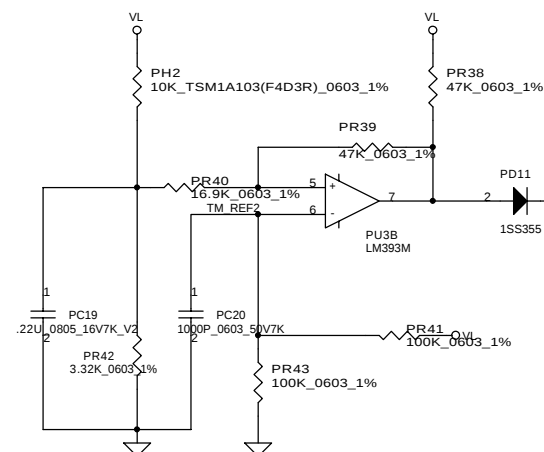
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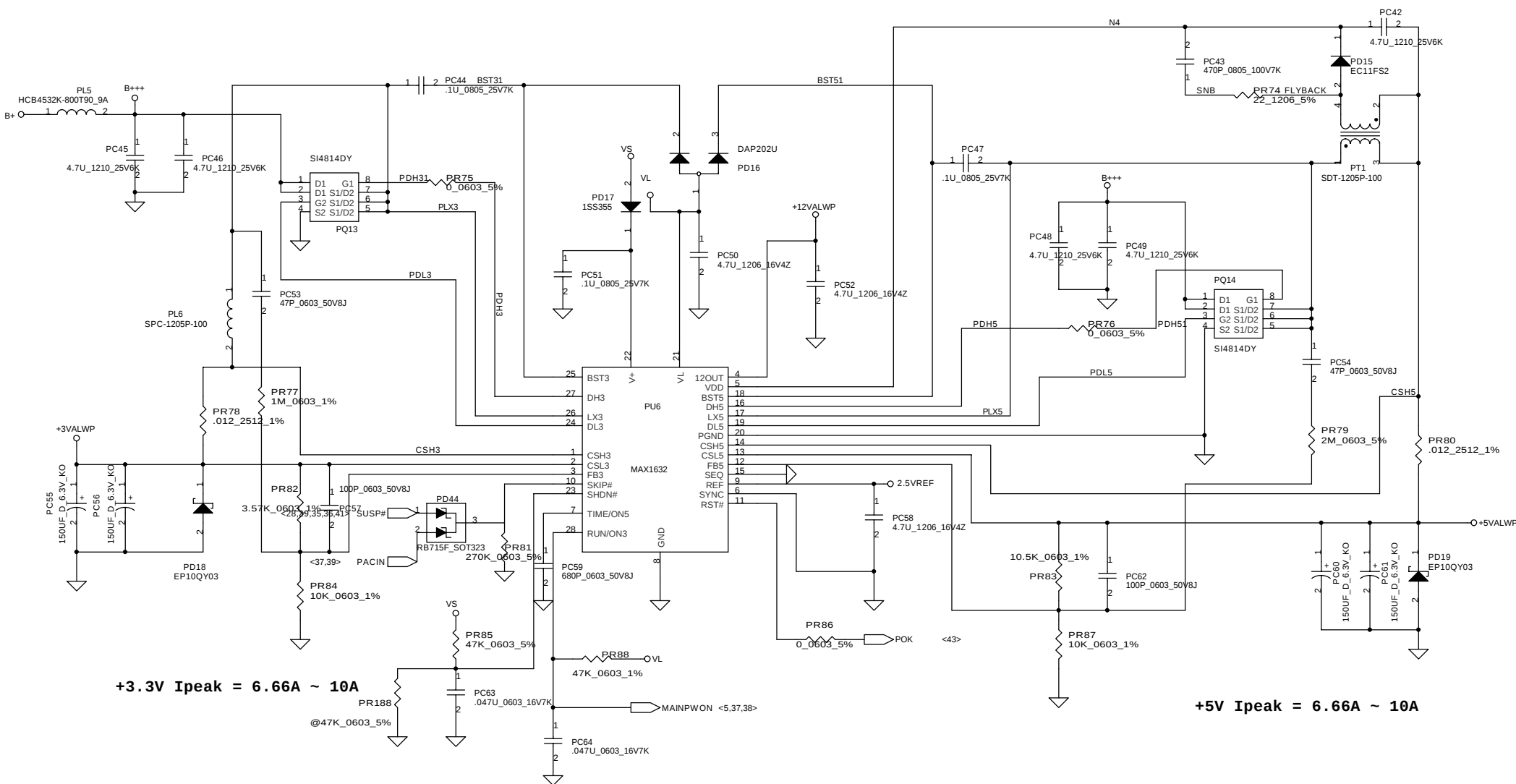


PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



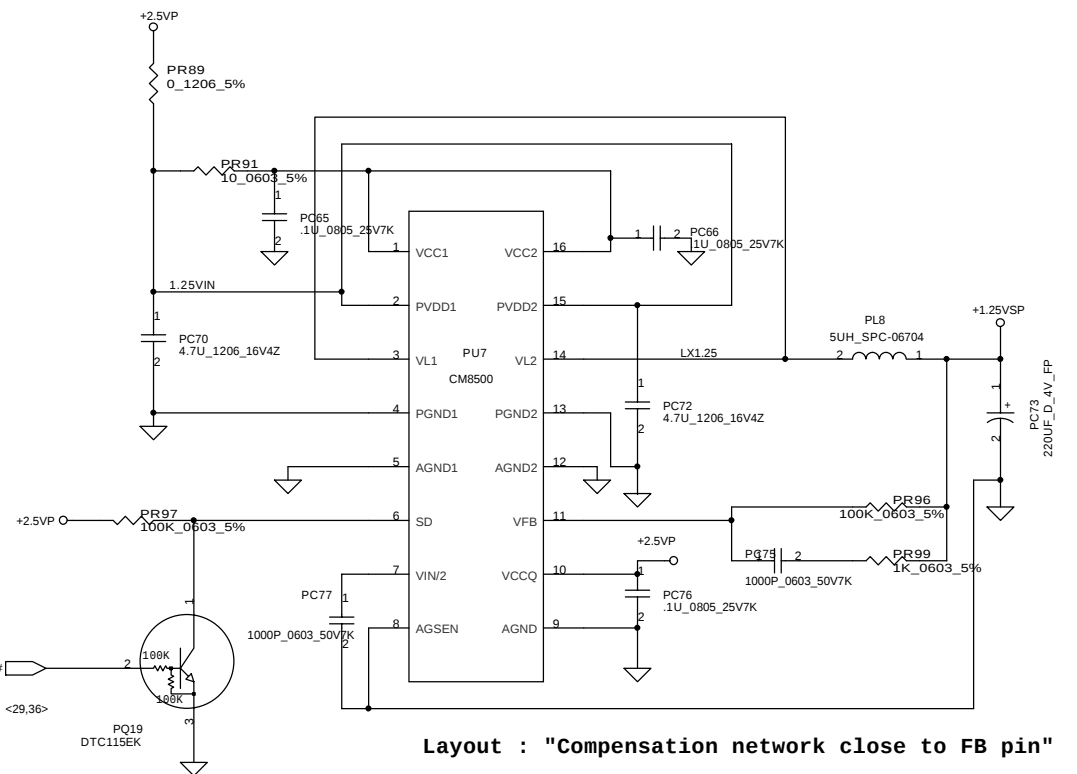
PH2 near main Battery CONN :
 BAT. thermal protection at 84 degree C
 Recovery at 45 degree C

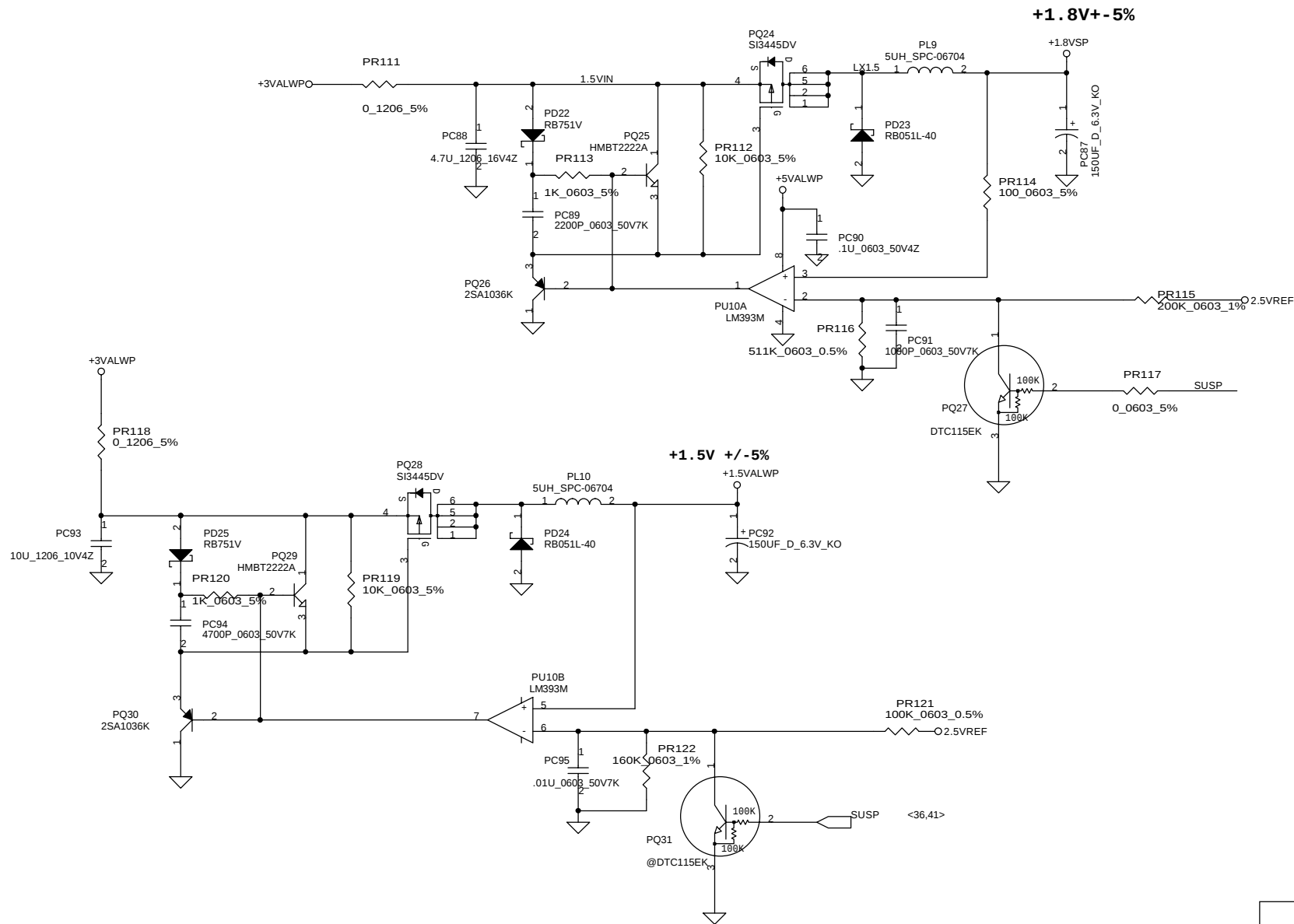




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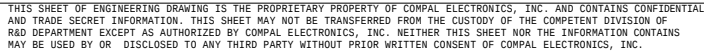
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
1		improve CPU core voltage drop	43	change PR149 from 3.9K_0603_1% to 3K_0603_1%	0.2
2		delete second battery component	38,44	delete PC142 , add PC16	0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Delete useless components	5	Delete Q7, Q8, Q11, R104, R116 and R117	0.2
			24	Delete C43 and C48	
			17	Delete D39	
2		Change BIOS ROM type	30	Delete U40, Add U41	0.2
3		Separate CD-ROM LED from Media LED	19	Delete U26 and C417, ADD R247	0.2
4		Delete second battery circuit	29	Delete C336; Pin 55, 82, 88, 156 of U42 change to be NC pin	0.3
5		For WNC wireless lan card only	34	Reserve R505 (un-populate)	0.3
6		Solve USB fail issue	17	Add R506	2.0

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Version change list (P.I.R. List)

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